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Subject: SiC Discrete Power Devices: ONR Contract N00014-1-0363: Final Report

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We wish you a Happy New Year.

Sincerely,

B. Jayant Baliga

Prof. B. Jayant Baliga
PSRC Director

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13. ABSTRACT *(Maximum 200 words)*

A novel planar vertical MOSFET structure, called ACCUFET, which eliminates both the problem of premature oxide breakdown and low inversion layer mobility has been demonstrated at Power Semiconductor Research Center.The contributions of the parasitic JFET regions in the ACCUFET to its forward conduction and forward blocking characteristics are discussed for the first time. A new process for fabrication of high voltage 4H-SiC ACCUFETs has been designed using insights gained. The process induced variations of the key design parameters of an ACCUFET are discussed. The fabrication of devices such as the Junction Barrier Schottky (JBS) diodes and the Junction Field Effect Transistors (JFET) is compatible with this process without the use of any additional mask levels or process steps. The forward conduction charactersitics of 4H-SiC ACCUFETs, fabricated on starting material with different epilayer doping and thickness values, are presented. The effect of the key design parameters such as the channel length, the buried JFET region width, and the gate oxide thickness, and the effect of their process-induced variations on the performance of these devices are discussed. Further, an analytical model developed previously for the on-resistance of the devices has been verified with the aid of the experimental results.

14. SUBJECT TERMS
ACCUFET, Schottky rectifier, specific on-resistance, breakdown voltage, Medici, JFET, MOSFET, FBSOA, drift region, inversion layer mobility, planar, Coulombic scattering, Gaussian profile, p-n junction

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Analysis of High Voltage 4H-SiC ACCUFET Operation

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Abstract

A novel planar vertical MOSFET structure (called ACCUFET), which eliminates both the problems of premature oxide breakdown and low inversion layer mobility, has been demonstrated by us. Here, the device physics and operation of the planar ACCUFET are discussed in detail. The contributions of the parasitic JFET regions in the ACCUFET to its forward conduction and forward blocking characteristics are discussed for the first time. Further, the effects of key device design parameters on device characteristics are described with the aid of two-dimensional simulations using *MEDICI*. In addition, an analytical model for evaluating the different components of the on-resistance of the planar ACCUFET is discussed here.

1.1 Introduction

Vertical MOSFETs fabricated from 4H-SiC are expected to show much lower specific on-resistance than those from 6H-SiC, due to a much higher (~10X) drift region electron mobility in 4H-SiC than in 6H-SiC. This makes 4H-SiC a very attractive material for high voltage devices. Our new fabrication run is aimed at making ACCUFETs on 4H-SiC starting material of varying epilayer thickness and doping values, which correspond to breakdown voltages ranging from 2000 V to 7500 V. The properties of the starting material for the high voltage devices are important for determining the device performance and for optimizing of device designs. In particular, when low doping starting material is used, which is typical of high voltage unipolar devices, the device behavior can be significantly altered. Hence, in order to develop good device designs, it is essential to understand the device physics to be able to predict the implications of the process and device design parameters on the device performance. Here, the device physics and operation of the planar ACCUFET are discussed in detail. The contributions of the parasitic JFET regions in the ACCUFET to its forward conduction and forward blocking characteristics are discussed for the first time. Further, the effects of key device design parameters on device characteristics are described with the aid of two-dimensional simulations using *MEDICI*. In addition, an analytical model for evaluating the different components of the on-resistance of the planar ACCUFET is discussed here.

1.2 Theory

The cross-section of a cell of the ACCUFET is shown in Fig. 1.1. The thickness and doping of the N- layer below the gate oxide is chosen such that it is completely depleted by the built-in potentials of the P^+/N^- junction and the MOS gate, resulting in a normally-off device with the entire drain voltage supported by the P^+/N^- drift junction. When a positive gate bias is applied, the electrons flow towards the drain through an accumulation channel created at the SiO_2/SiC interface. The electrons flowing out of the source need to pass through a MOS channel at the surface, a parasitic buried JFET region, and the drift region before reaching the drain. There is also a parasitic surface JFET in the ACCUFET structure near the channel that can effect the blocking characteristics of the device. In order to understand the operation of the ACCUFET, it is important to review the device physics of JFETs, MOS transistors and the drift region in vertical unipolar devices, which are discussed in this section.

1.2.1 JFET

1.2.1.1 Basic Device Characteristics

Fundamentally, the Junction Field Effect Transistor (JFET) consists of a bar of semiconductor material whose resistance can be controlled by the application of a reverse bias voltage to a gate region [1]. Fig. 1.2 presents the structures of high voltage JFETs with gates located at the surface and with gates buried under the source regions. In the absence of a gate bias, the current flow between drain and source is limited by the resistance of the lightly doped N-type region between these current carrying terminals. The N-type region consists of two portions. The region between the junction gates is

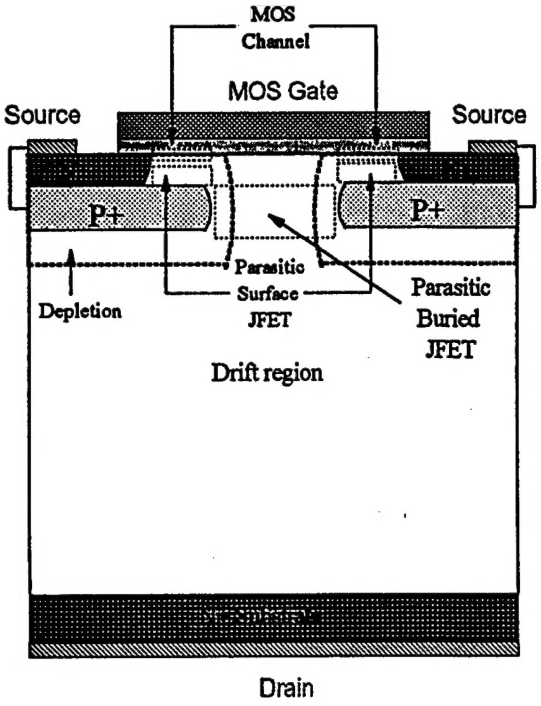


Fig. 1.1 Cross-section of an ACCUFET exhibiting the MOS channel and the parasitic JFET regions.

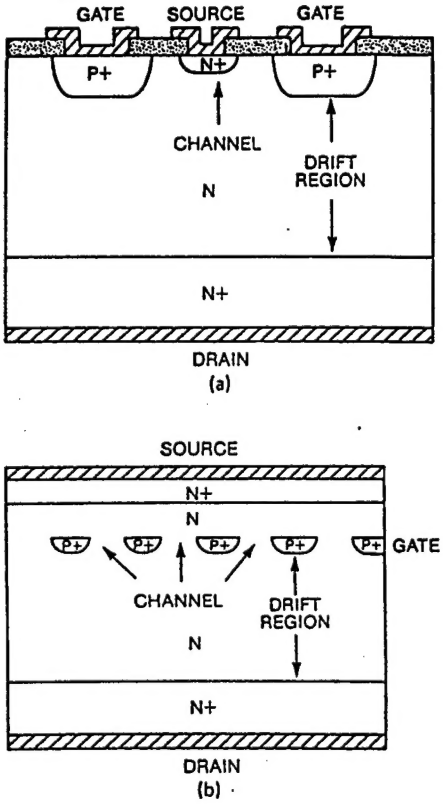


Fig. 1.2 Structures of high voltage JFETs with gates located at (a) at the surface and (b) buried below the source region.

called the channel and the region below the gates is called the drift region. With the application of a reverse gate bias with respect to the source, a depletion layer forms around the gate junctions and extends out into the channel. Since the depletion region is devoid of free carriers, the resistance of the channel region increases with the application of higher reverse gate voltages. Thus, the JFET is a voltage controlled device in which the current through its channel can be controlled by varying the gate voltage.

In the forward blocking mode, the depletion layers from the gate junctions extend through the entire channel. The applied reverse gate bias sets up a potential barrier in the channel. For current to flow between drain and source, electrons must surmount this potential barrier. As the drain voltage increases, the potential barrier is lowered and electron injection becomes easier.

1.2.1.2 Types of JFETs

Based on device behavior, the JFETs could be classified into two categories: long-channel and short-channel JFETs. The long-channel JFETs exhibit pentode-like current-voltage characteristics, that is the drain current saturates at large drain voltages. In the long-channel devices, the length of the gate along the current flow path is much larger than the channel width (Fig. 1.3). At small drain voltages, the depletion width is determined by the gate voltage. It extends with uniform width across the gate junction. When the drain voltage becomes comparable to the gate voltage in the presence of a substantial vertical drain-source current flow, a large drop in voltage occurs across the channel. Then, the depletion layer progressively widens from the source towards the drain. The channel width is then smaller on the drain side, which increases the resistance to the current flow. The resultant pentode-like characteristics are shown in Fig. 1.4. Current saturation occurs at high drain voltages when the adjacent gate depletion layers intersect in the channel.

In the long-channel devices, the drain potential cannot penetrate into the channel. However, if the gate structure is designed with a small channel length compared with the channel width, the JFET characteristics are significantly altered. In the short channel structure, the potential barrier established in the channel by the reverse gate bias extends over only a small vertical distance (Fig. 1.5). As the drain voltage is increased, the drain potential penetrates into the channel and lowers the potential barrier, which in turn allows electron injection to occur. Since the injection of carriers across the potential barrier varies exponentially with the barrier height, the drain current exhibits a rapid increase once the potential barrier is reduced. The resultant triode-like characteristics, that is, drain current continuously increasing with increasing drain voltage, are shown in Fig. 1.6.

1.2.1.3 Forward Conduction

The fundamental structure of the gate (channel) region in a JFET in shown in Fig. 1.7. The current flow between the drain and source contacts is carried by majority carriers in the channel region. When a reverse bias is applied to the gate with respect to the source, the gate junction depletion layer extends into the channel region, reducing its cross-sectional area. This allows the modulation of the drain current by the means of the applied gate voltage. The depletion layer widths can be determined by using expressions

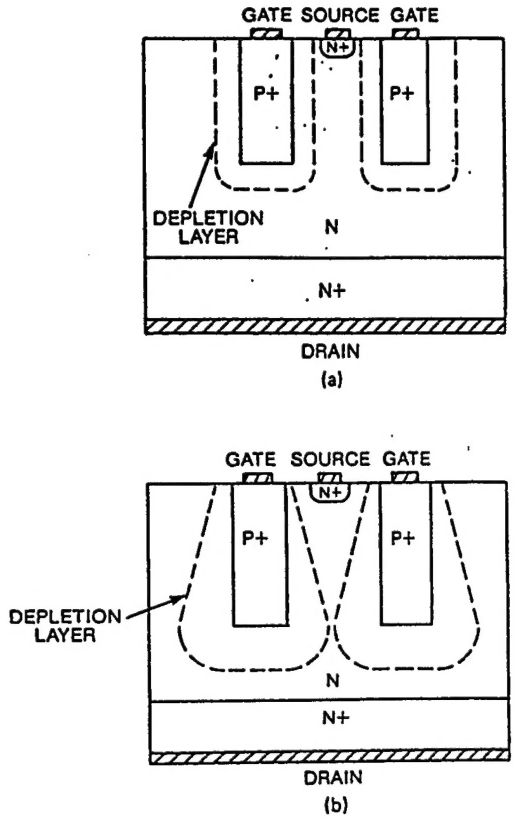


Fig. 1.3 Long-channel JFET structure operating at (a) low and (b) high drain voltage.

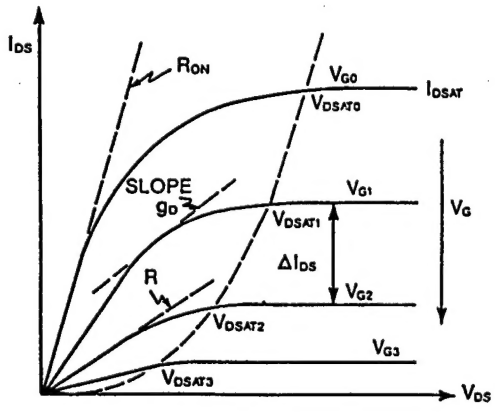


Fig. 1.4 Pentodelike characteristics of a long-channel JFET.

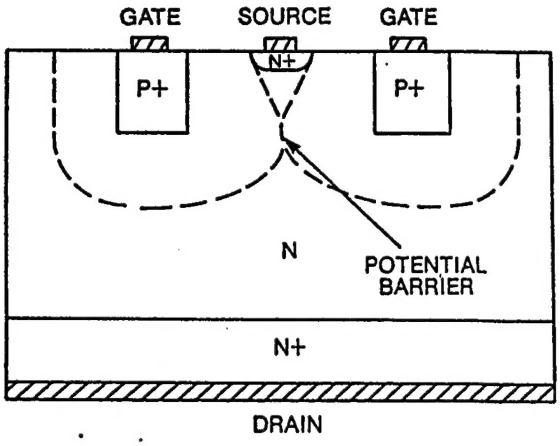


Fig. 1.5 Short-channel JFET structure.

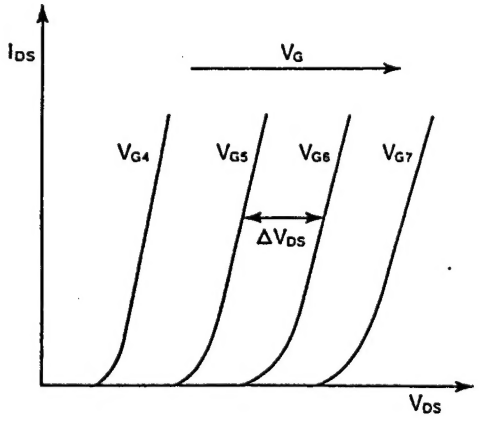


Fig. 1.6 Triodelike characteristics of short-channel JFET.

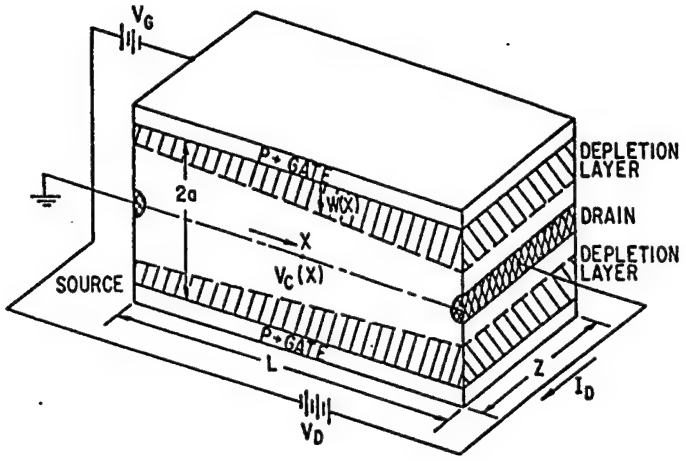


Fig. 1.7 Fundamental structure of a JFET in the gate region.

for the reverse-bias junction voltages of V_G and (V_G + V_D). In the case of a uniformly doped channel with a doping density of N_D per cubic centimeter, the depletion layer widths at the source and the drain ends of the channel are given, respectively, by

$$W_S = \sqrt{\frac{2\varepsilon_s(V_G + V_{bi})}{qN_D}} \tag{1.1}$$

and

$$W_D = \sqrt{\frac{2\varepsilon_s(V_D + V_G + V_{bi})}{qN_D}} \tag{1.2}$$

where the absolute values of the gate (V_G), drain (V_D) and the built-in (V_{bi}) potentials must be used in the equations. The junction built-in potential is given by

$$V_{bi} = \frac{kT}{q} ln\left(\frac{N_D N_A}{n_i^2}\right) \tag{1.3}$$

where, N_A and N_D are the doping concentrations on the opposite sides of the abrupt metallurgical junction.

The current flow in the channel of the JFET can be derived analytically by making two additional assumptions: (1) the mobility is constant, and (2) the magnitude of the electric field along the channel (i.e. the longitudinal field) is much smaller than the electric field normal (i.e. the transverse field) to the channel - this is termed the *gradual channel approximation*. This allows a one-dimensional calculation of the depletion width of the gate junction after taking into account the local potential in the channel. This approximation is good one for the devices with large length to width (L/*a*) ratios.

Assuming an abrupt gate junction, the depletion width at location x along the channel is given by

$$W(x)=\sqrt{\frac{2\varepsilon_s(V_C(x)+V_G+V_{bi})}{qN_D}} \tag{1.4}$$

where V_C is the local potential in the channel at location x. The channel cross-section at x is $2[a - W(x)]$. From this cross section and the conductivity, the drain current can be obtained as

$$I_D=2[a-W(x)](q\mu n_D)Z\left(\frac{dV}{dx}\right) \tag{1.5}$$

where a is half the width of the undepleted channel, and n_D is the majority carrier concentration in the undepleted channel. Further, differentiation of Eq. (1.4) gives

$$dV=\frac{qN_D}{\varepsilon_s}WdW \tag{1.6}$$

By using Eq. (1.6) in Eq. (1.5) and integrating from x=0 to x=L, and then by using Eqs. (1.1) and (1.2), it can be shown that

$$I_D=2a(q\mu n_D)\frac{Z}{L}\left\{V_D-\frac{2}{3a}\left(\frac{2\varepsilon_s}{qN_D}\right)^{1/2}\left[(V_D+V_G+V_{bi})^{3/2}-(V_G+V_{bi})^{3/2}\right]\right\} \tag{1.7}$$

The output current-voltage characteristics of the JFET in the pentode regime (Fig. 1.4) can be obtained from this equation.

In the linear region of the output characteristics, the JFET exhibits a resistive characteristic, with the resistance a function of the gate bias voltage. This resistance can be obtained by differentiating Eq. (1.7) with respect to the drain voltage:

$$\frac{1}{R}=\frac{dI_D}{dV_D}=2(q\mu n_D)\frac{Z}{L}\left\{a-\sqrt{\frac{2\varepsilon_s(V_D+V_G+V_{bi})}{qN_D}}\right\} \tag{1.8}$$

Since the drain voltage V_D is much smaller than the gate voltage V_G in the linear region, it follows that

$$R=\frac{L}{2q\mu n_D(a-W_S)} \tag{1.9}$$

The resistance in the linear region given by Eq. (1.9) is simply equal to that of semiconductor region of width $2(a\text{-}W_S)$.

As the drain voltage increases, the depletion layer width W_D on the drain end of the channel also increases in size. The channel is pinched off when this depletion width extends to half the channel width. The condition for pinch-off can be represented by

$$V_P=(V_D+V_G+V_{bi})=\frac{qN_Da^2}{2\varepsilon_s} \tag{1.10}$$

where V_p is called the pinch-off voltage. The drain current increases with the drain voltage until the pinch-off condition occurs, after which the drain current becomes constant. The saturation drain current can be obtained from Eqs. (1.7) and (1.10) as

$$I_{D,sat} = 2a(q\mu n_D)\frac{Z}{L}\left\{\frac{qN_Da^2}{6\varepsilon_s} - (V_G + V_{bi}) + \frac{2}{3a}\left(\frac{2\varepsilon_s}{qN_D}\right)^{1/2}(V_G + V_{bi})^{3/2}\right\} \quad (1.11)$$

1.2.1.4 Forward Blocking

It was shown in the previous section that in the forward conduction mode, the JFETs exhibit pentode-like characteristics. In the forward blocking mode, the JFETs exhibit triode-like characteristics, controlled by the presence of a potential barrier in the channel. When the depletion layers from the gates extend enough to intersect at the channel, a potential barrier is formed, and the transport of the electrons from source to drain is controlled by the injection of carriers over the potential barrier.

The effect of changes in the gate and drain voltages on the potential barrier height are illustrated in Fig. 1.8. For a fixed drain voltage (Fig. 1.8(a)), as the gate voltage increases, a potential barrier is formed after the pinch-off condition is reached. Further increase in the gate voltage results in a proportional increase in the barrier height. The drain voltage has an opposite influence as shown in Fig. 1.8(b). For a fixed gate voltage, as the drain voltage increases, the barrier height is reduced by the penetration of the drain potential into the channel.

As may be expected, the geometric shape of the channel and its doping level influence the modulation of the potential barrier by the gate and drain voltages. The effect of changing the gate length[2] is shown in Fig. 1.9. The potential distribution shown here is based on two-dimensional numerical analysis. Note that for the case of a small gate length, the potential barrier reduces rapidly with the increasing drain potential. The numerical analysis also indicates that a smaller channel width will result in an increase in the potential barrier height.

The current flow in a JFET operating in the triode regime can be limited by the injection of carriers across the channel potential barrier. It can be described by the equation

$$I_D = I_0 e^{-(qV_B/kT)} \quad (1.12)$$

where V_B is the height of the channel potential barrier. To relate the drain current to the drain and gate voltages, it is necessary to perform a numerical analysis including the two dimensional potential distribution.

1.2.2 MOSFET

1.2.2.1 Basic Operation

The basic Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is illustrated in Fig. 1.10, for the case of an n-type channel formed on a p-type Si substrate [3]. The N+ source and drain regions are diffused or implanted into a relatively lightly doped p-type substrate, and a thin oxide layer separates the Al metal gate from the Si surface. No current flows from drain to source without a conducting n-channel between them, since the drain-substrate-source combination includes oppositely directed p-n-junctions in series. When a positive voltage is applied to the gate relative to the substrate (which is connected to the source in this case), negative charges are induced in the

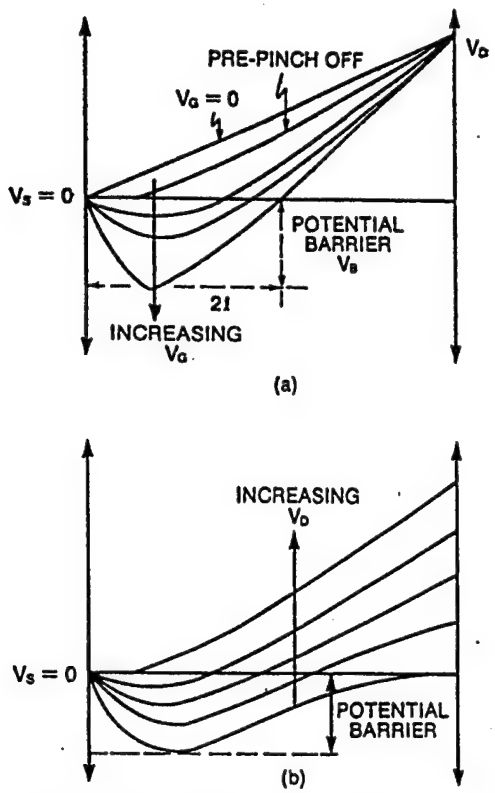


Fig. 1.8 Effect of gate and drain voltages on the channel potential barrier height.

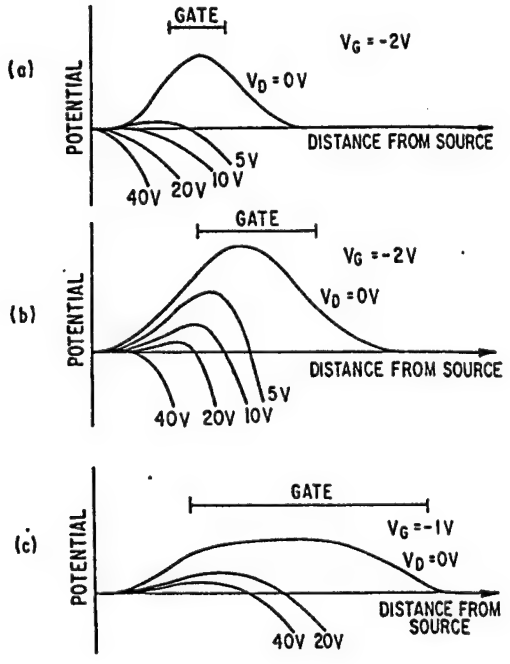


Fig. 1.9 Effect of increasing gate length on the channel potential barrier reduction by the drain voltage.

underlying Si, by the formation of a depletion region and a thin surface region containing mobile electrons. These induced electrons form the channel of the FET and allow current to flow from drain to source. The effect of the gate voltage is to vary the conductance of this induced channel for low drain-to-source voltage. As the drain-to-source voltage is increased, the channel gets pinched-off and the drain current saturates at essentially a constant value. An important parameter in MOS transistors is the threshold voltage V_T, which is the minimum gate voltage required to induce the channel.

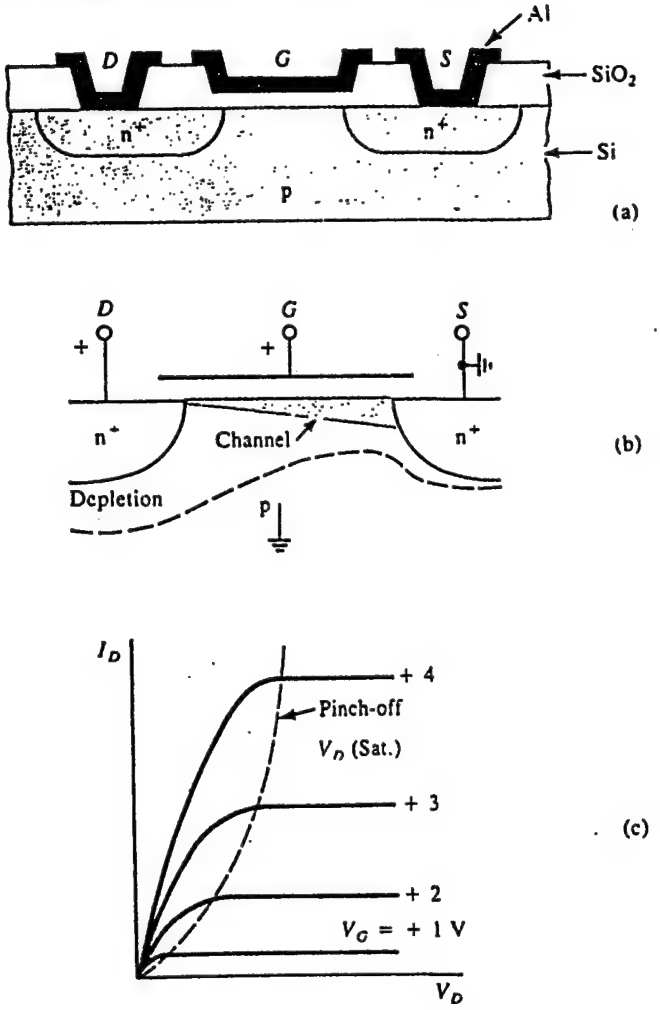


Fig. 1.10 An n-channel MOS transistor: (a) device cross section; (b) schematic illustration of the induced n-channel and the depletion region near pinch-off; (c) drain current-voltage characteristics as a function of gate voltage.

1.2.2.2 Forward Conduction

The current flow between source and drain is controlled by the electron charge available for transport in the surface channel (inversion) layer of the p-type region as well as the surface mobility of these electrons. According to the MOS analysis, when the surface potential (ψ_s) exceeds twice the bulk potential (ψ_B), a strong inversion layer begins

to form [1]. Since the band bending is small beyond this point, the inversion layer charge available for current conduction is given by

$$Q_n = C_{ox}(V_G - V_T) \tag{1.13}$$

where, C_{ox} is the gate oxide capacitance, V_G is the gate voltage and V_T is the threshold voltage. Thus, the channel resistances at low drain voltages, where the voltage drop along the channel is negligible, is given by

$$R_{ch} = \frac{L}{Z\mu_{ns}C_{ox}(V_G - V_T)} \tag{1.14}$$

where Z and L are the width and the length of the channel and μ_{ns} is the surface mobility of electrons. The surface mobility is an important parameter in determining the conductance of the channel in a MOSFET and is discussed in detail in the next section.

The channel resistance can be derived as a function of the gate and drain voltages under the following assumptions:

1. the gate structure is an ideal MOS structure, which is defined as one that satisfies the following conditions:
   (a) the insulator has infinite resistivity,
   (b) charge can exist only in the semiconductor and on the metal electrode,
   (c) there is no energy difference between the work function of the metal and the semiconductor, which results in no band bending (*flatband condition*) in the absence of a gate bias.
2. the free carrier mobility is a constant independent of the electric field strength,
3. the p-type (base) region is uniformly doped,
4. the current transport occurs exclusively by drift,
5. the leakage current is negligible,
6. the longitudinal electric field along the surface is small compared with the transverse electric field resulting from the gate bias (also referred to as *gradual channel approximation*).

The resistance (dR) of an elemental segment (dy) of the channel is dependent upon the inversion layer charge per unit area and the mobility of the free carriers:

$$dR = \frac{dy}{Z\mu_{ns}Q_n(y)} \tag{1.15}$$

The charge in the inversion layer not only depends upon the gate voltage but also depends on the drain current because of the potential drop across the channel:

$$Q_n(y) = C_{ox}[V_G - V_T - V(y)] \tag{1.16}$$

where V(y) is the voltage drop along the channel. The voltage drop in the segment dy is then given by:

$$dV = I_D dR \tag{1.17}$$

Hence,

$$\int_0^L I_D dy = -Z\mu_{ns}C_{ox}\int_0^{V_D}(V_G - V_T - V)dV \tag{1.18}$$

If the drain current (I_D) is assumed to remain constant throughout the channel, then:

$$I_D = \frac{\mu_{ns} C_{ox} Z}{2L}\left[2(V_G - V_T)V_D - V_D^2\right] \tag{1.19}$$

When the drain voltage is small, the drain current increases linearly with drain voltage:

$$I_D = \frac{\mu_{ns} C_{ox} Z}{L}(V_G - V_T)V_D \tag{1.20}$$

In this linear region, the channel resistance is given by:

$$R_{ch} = \frac{L}{Z\mu_{ns} C_{ox}(V_G - V_T)} \tag{1.21}$$

which agrees with the expression given in Eq. (1.14) representing a homogenous inversion layer extending between drain and source.

As the drain voltage increases, there is a reduction in the channel inversion layer charge near the drain. Ultimately, the inversion layer charge at the drain end of the channel becomes zero and the drain current saturates. The drain voltage at which the current saturation occurs is the channel pinch-off point :

$$V_{DS} = (V_G - V_T) \tag{1.22}$$

The saturation drain current is obtained by using Eq. (1.22) into (1.19):

$$I_{DS} = \frac{\mu_{ns} C_{ox} Z}{2L}(V_G - V_T)^2 \tag{1.23}$$

The saturation current is an important parameter because it determines the maximum current that the channel will transport. The *transconductance* of the device in the saturated current region of operation can be obtained by differentiating Eq. (1.23) with respect to the gate voltage :

$$g_{ms} = \frac{dI_D}{dV_G} = \mu_{ns} C_{ox} \frac{Z}{L}(V_G - V_T) \tag{1.24}$$

1.2.2.3 Short Channel Effects

When the channel length in a MOS transistor is made very small, the saturation current does not remain constant with increasing V_D, but instead it increases. This is because in deriving Eq. (1.23), it was assumed that the channel length L was not changed beyond pinch-off by the increasing drain potential. However, for short channels, the spreading of the depletion at the drain significantly reduces the effective channel length (L') as shown in Fig. 1.11. This is referred to as *channel length modulation*. The reduction in the channel length, ΔL, can be a function of several parameters [4]. By assuming that the field in the depletion region near the surface is approximately horizontal, it can be shown by using Poisson's equation that the length ΔL of the depletion region can be related to the potential (V_{DS} - V'_{DS}) across it by

$$\Delta L = \sqrt{\frac{2\varepsilon_s}{qN_A}}\left[\sqrt{\phi_D + (V_{DS} - V'_{DS})} - \sqrt{\phi_D}\right] \tag{1.25}$$

where

$$\phi_D = \frac{\varepsilon_s E_1^2}{2qN_A} \tag{1.26}$$

where N_A is the substrate concentration and E_1 is an electric field value above which the electron velocity is assumed saturated.

The effect of decreasing L is to deplete more of the region under the inversion layer. The deeper depletion region is accompanied by a larger surface potential (*barrier lowering*), which makes the channel more attractive for the electrons. Thus, the device can conduct more current than what would be predicted from long-channel theory for a given V_{GS}. Since, in the long-channel theory, the drain current is an increasing function of V_{GS}-V_T, the long channel equations may be made to describe artificially the current increase if V_T is replaced by a smaller quantity V'_T, which is called the *effective threshold*. The effective threshold voltage is affected by several factors [4] as summarized here:

The effective threshold voltage *decreases* when:

1. the substrate doping *decreases*.
2. the oxide thickness *decreases*.
3. the channel length *decreases*.
4. the channel width *increases*.
5. the junction depth *increases*.

1.2.2.4 Surface Mobility

The transport of free carriers near the surface is of importance to MOSFETs. The conductivity of the inversion and accumulation layers is dependent upon the total number of free carriers in the layer and their transport velocity along the surface under an applied transverse electric field. A pictorial representation of a semiconductor surface containing an inversion layer is shown in Fig. 1.12. In addition to Coulombic scattering due to ionized acceptors, the electrons in the inversion layer undergo several additional scattering processes:

1. surface phonon scattering due to lattice vibration : phonon scattering is important at higher temperatures when the thermal energy in the lattice is large.
2. additional Coulomb scattering due to surface charge in interface states and the fixed oxide charge : this is important when processing conditions produce high interface state or fixed charge densities.
3. surface roughness scattering due to deviation of the surface from a specular interface : this effect is predominant when the electric field normal to the surface is large, e.g. under strong inversion conditions.

It is useful to define an effective mobility for carriers in the inversion layer:

$$\mu_e = \frac{\int_0^{x_i} \mu(x) n(x) dx}{\int_0^{x_i} n(x) dx} \tag{1.25}$$

where $\mu(x)$ and $n(x)$ are the local mobility and free carrier concentrations, respectively, in the inversion layer, and x_i is the inversion layer thickness. Defined in this manner, the effective mobility is a measure of the conductance of the inversion layer, so that this

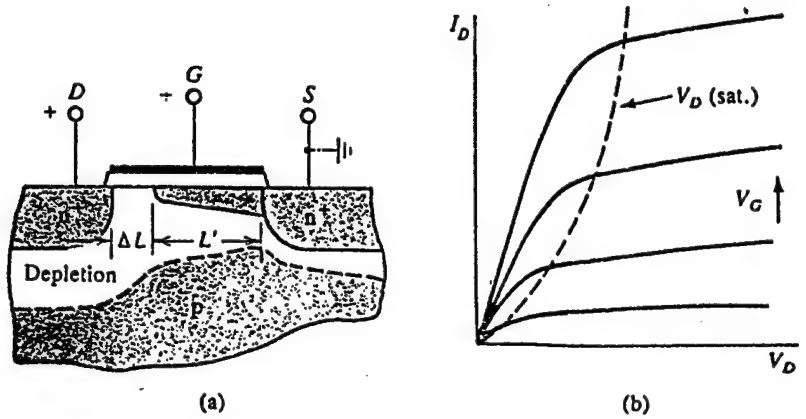


Fig. 1.11 Short-channel effects: (a) reduction of the effective channel length in saturation; (b) increase in drain current beyond pinch-off due to channel length modulation.

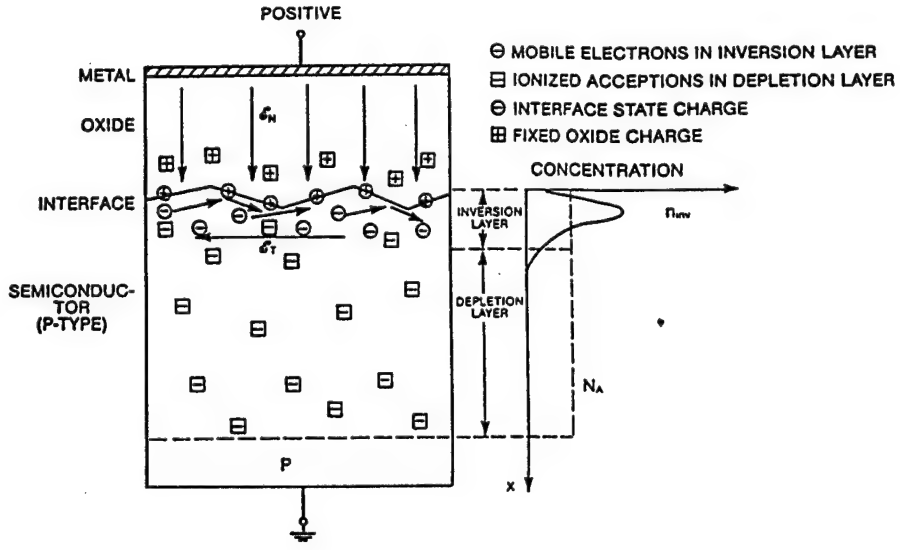


Fig. 1.12 Metal-oxide-semiconductor surface with inversion layer.

concept is eminently suitable for the calculation of characteristics of MOS field effect devices. In fact, determination of the effective mobility is performed by using MOSFET devices. The effective mobility has been found to decrease with increase in substrate doping concentration and the charge at the oxide interface.

When the direction of the electric field normal to the surface is such as to attract the majority carriers to the surface, an accumulation layer forms. The carriers in the accumulation layer are distributed further from the surface than in the case of inversion layers. Because of this, the effective mobility in an accumulation layer can be expected to be higher than in an inversion layer because surface roughness scattering is not as severe.

1.2.3 Drift Region

The high voltage power MOSFETs contain a drift region, which is designed to support the high applied voltage between drain and source during forward blocking. To provide the high blocking voltage capability, the drift region must be lightly doped. Its resistance has a strong influence on the on-resistance of the high voltage MOSFETs because the drain current must flow through the drift region.

To analyze the influence of the drift region on drain current flow, consider the cross-section of a planar ACCUFET cells illustrated in Fig. 1.13. In these figures, the depletion region is showed by the dashed lines. It is assumed that the current transport occurs exclusively from the surface channel through the undepleted JFET region (of width, *b*) and then spreads through the drift region at an angle β, as illustrated. For a fixed cell width, the current distribution can have two profiles depending on the thickness of the epilayer. In the case of a thin epilayer, as shown in Fig. 1.13(a), the current is still spreading when it reaches the substrate. In thick epilayers, the current is able to spread completely and then, flow with a uniform distribution (Fig. 1.13 (b)). The expressions for the drift region specific on-resistance in the two cases are derived here.

The resistance of a segment *dy* located at a distance *y* from the JFET region is given by

$$dR(y) = \frac{dy}{q\mu_n n_D Z(2t)} \tag{1.26}$$

where, μ_n is the bulk mobility of the majority carriers in the c-axis direction, n_D is the carrier concentration, and $2t(y)$ is the width of the current flow path at point *y* in the drift region. From Fig. 1.13, it can been seen that

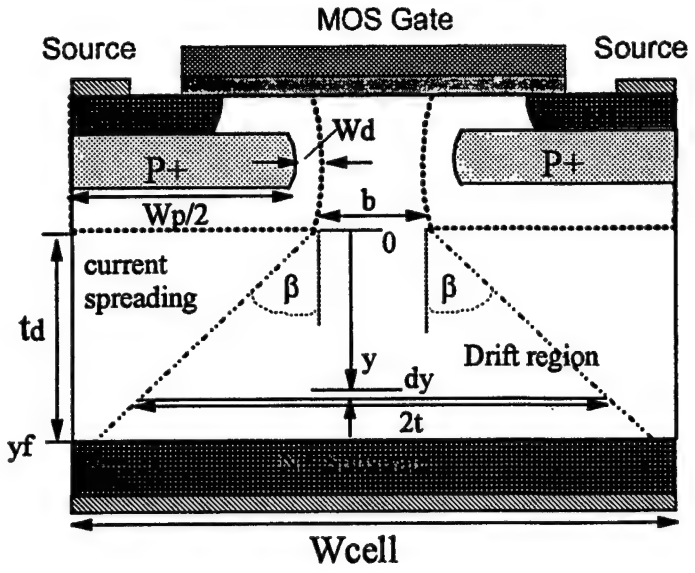
$$2t(y) = b + 2y\tan\beta \tag{1.27}$$

If the current is assumed to be spreading between $y=0$ and $y=y_f$, the drift region resistance in the region where the current spreads can be obtained by integrating Eq. (1.26) as follows

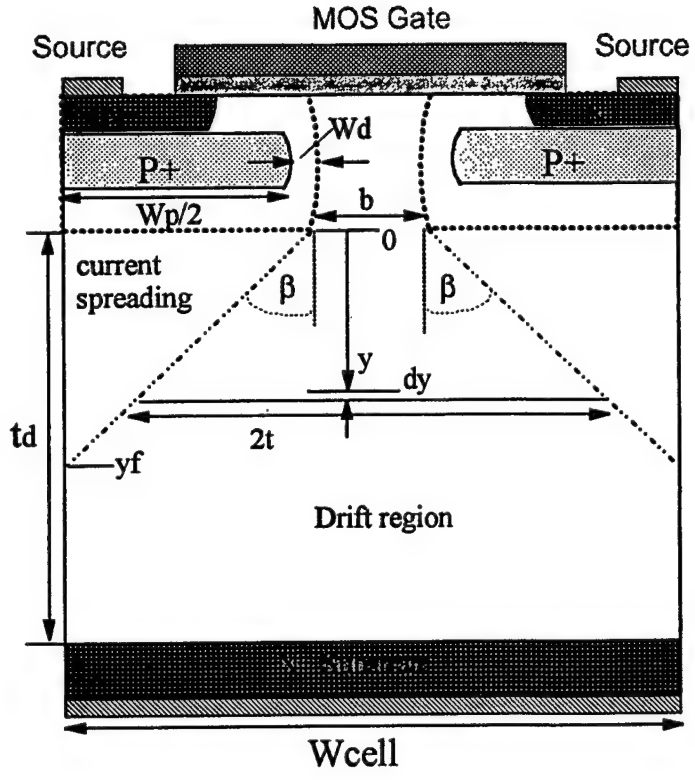
$$\int_0^{Rs} dR = \int_0^{y_f} \frac{dy}{q\mu_n n_D Z(b + 2y\tan\beta)} \tag{1.28}$$

Hence,

$$Rs = \frac{1}{q\mu_n n_D Z(2\tan\beta)} ln\left[1 + \frac{2y_f \tan\beta}{b}\right] \tag{1.29}$$



(a)



(b)

Fig. 1.13 Drift region resistance modeling for (a) thin and (b) thick epilayers.

Depending on the thickness of the epilayer and the cell width, two cases can be analyzed.

Case I :

The current spreading in the epilayer is incomplete when t_d (thickness of the drift region) satisfies the criterion:

$$td < \frac{(W_p + 2W_d)}{2\tan\beta} \tag{1.30}$$

where, W_p is the width of the buried P+ layer in the cell, and W_d is the width of depletion region in the JFET region near the buried P+ layer. Assuming that p-n junction at the JFET region is an abrupt junction in which the doping of the p-region is much higher than that of the n-type region, W_d is given by

$$W_d = \sqrt{\frac{2\varepsilon_s(V_{bi})}{qN_D}} \tag{1.31}$$

where, the junction built-in potential is given by

$$V_{bi} = \frac{kT}{q} ln\left(\frac{N_D N_A}{n_i^2}\right) \tag{1.32}$$

In this case, using $y_f = t_d$ in Eq. (1.29) gives the on-resistance of the drift region, R_d, as

$$R_d = \frac{1}{q\mu_n n_D Z(2\tan\beta)} ln\left[1 + \frac{2t_d \tan\beta}{b}\right] \tag{1.33}$$

Case II:

The current is able to spread completely in the epilayer and flow uniformly thereafter, when t_d satisfies the criterion:

$$td > \frac{(W_p + 2W_d)}{2\tan\beta} \tag{1.33}$$

In this case, Eq. (1.26) can describe the current flow only until

$$y = \frac{(W_p + 2W_d)}{2\tan\beta} = y_f \tag{1.34}$$

Hence, the on-resistance of the drift region consists of two components. The first component (R_s) is due to the region in which the current spreads, which can be obtained by using Eq. (1.34) in Eq. (1.29) :

$$Rs = \frac{1}{q\mu_n n_D Z(2\tan\beta)} ln\left[1 + \frac{W_p + 2W_d}{b}\right] \tag{1.35}$$

The second component (R_u) is due to the region of thickness (t_d-y_f) in which the current flow is uniform. Hence,

$$R_u = \frac{\left(t_d - \frac{W_p + 2W_d}{2\tan\beta}\right)}{q\mu_n n_D Z W_{cell}} \tag{1.36}$$

The drift region specific on-resistance ($R_{d,sp}$) in this case can be obtained by multiplying the drift region on-resistance with $W_{cell}Z$. Thus,

$$R_{d,sp} = \frac{W_{cell}}{q\mu_n n_D (2\tan\beta)} ln\left[1 + \frac{W_p + 2W_d}{b}\right] + \frac{\left(t_d - \frac{W_p + 2W_d}{2\tan\beta}\right)}{q\mu_n n_D} \tag{1.37}$$

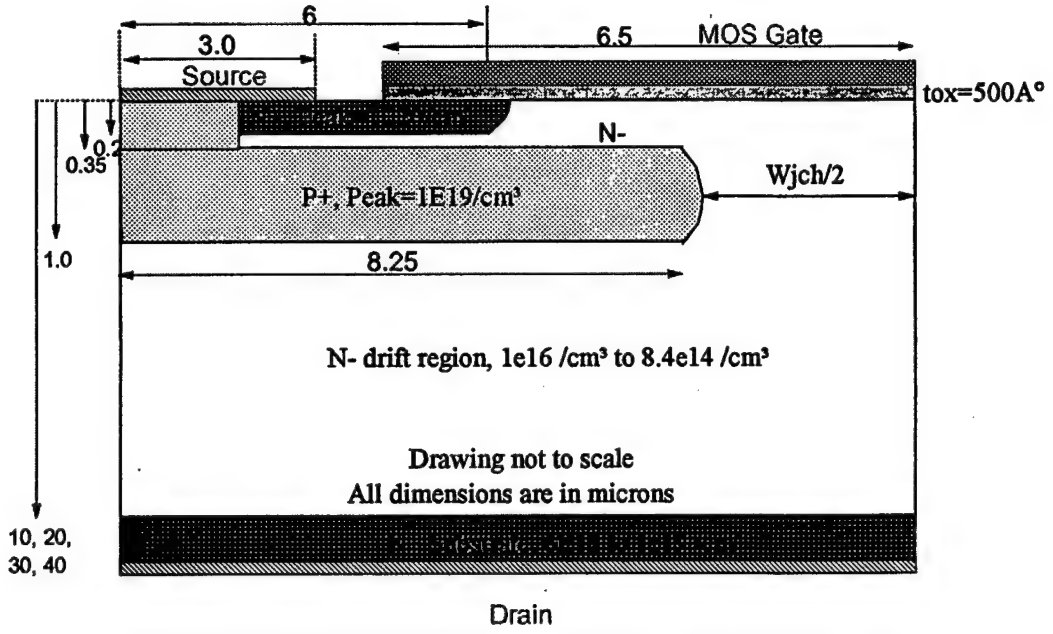


Fig. 1.14 Schematic of the 4H-SiC ACCUFET cell used in simulations.

1.3 ACCUFET Structure and Operation

The cross section of the 4H-SiC ACCUFET half-cell used in the simulations is shown in Fig. 1.14. The thickness and doping of the N- layer below the gate oxide is chosen such that it is completely depleted by the built-in potentials of the P^+/N^- junction and the MOS gate, resulting in a normally-off device with the entire drain voltage supported by the P^+/N^- drift junction. The device is expected to have high breakdown voltage as this implanted P^+/N^- junction can support high voltages. The structure also utilizes the buried P^+ region to suppress the electric field below the gate oxide, thereby preventing oxide rupture. When a positive gate bias is applied, the electrons flow through an accumulation channel created at the SiO_2/SiC interface. Since the accumulation layer mobility is expected to be higher than the inversion layer mobility, a lower on-resistance is expected for this device.

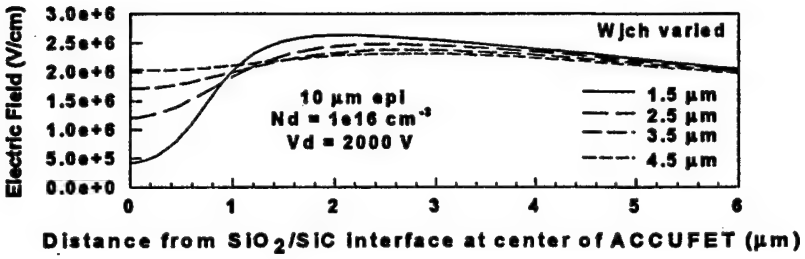
The device characteristics of the planar ACCUFET were studied by simulations performed using *MEDICI* on four different starting materials. The epilayer thickness values were chosen to be 10 μm, 20 μm, 30 μm and 40 μm. The epilayer (drift region) doping was chosen to be $1x10^{16}$ cm^{-3}, $2.1x10^{15}$ cm^{-3}, $2.5x10^{15}$ cm^{-3}, and $8.4x10^{14}$ cm^{-3}, respectively, based on the available starting material. The substrate doping, similarly, was $1x10^{19}$ cm^{-3}, $6x10^{18}$ cm^{-3}, $7.8x10^{18}$ cm^{-3}, and $8.6x10^{18}$ cm^{-3}, respectively. The substrate thickness was 2 μm in all cases. The N+ source was 0.2 μm deep, and had a Gaussian doping profile with a peak concentration of $1x10^{20}$ cm^{-3}. The buried P+ layer was also chosen to have a Gaussian profile with a peak concentration of $1x10^{19}$ cm^{-3} at depth of 0.65 μm. The layer formed a P+/N- junction at a depth of 1 μm, and chosen to be 16.5 μm wide (W_p). The JFET region width (W_{jch}), which is the distance between adjacent buried P+ layers, was varied from 1.5 μm to 1.5 μm. These values were selected based on practical cell designs that could be fabricated based on design rules for the photolithography equipment available in the NCSU AEMP cleanroom. The channel length (L_{ch}) was varied from 1.25 μm to 1.25 μm. The gate oxide was chosen to be 500 Å thick. Both the N+ source and the buried P+ regions were connected to the same electrode and maintained at ground potential during simulations.

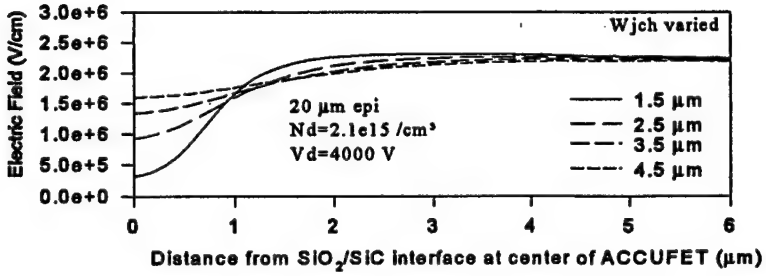
As described earlier, the planar ACCUFET has been conceived to take care of the problems of low inversion layer mobilities and premature oxide breakdown, which are two very important issues for silicon carbide devices. In the following sections, the effects of critical design parameters on the electric field distribution and the current-voltage characteristics are discussed.

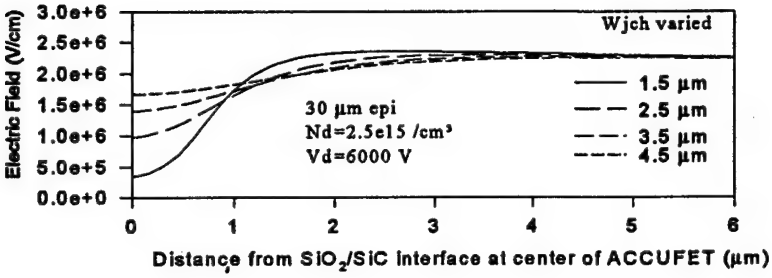
1.3.1 Electric Fields

1.3.1.1 Effect of JFET width

The JFET region width (W_{jch}) in the ACCUFET, which is the distance between two adjacent buried P+ layers, is an important design parameter. When a large drain bias is applied, the JFET region is pinched off. This shields the region above the JFET region from the high drain voltage by creating a potential barrier as discussed in section 1.1.2.1. This reduces the electric field near the SiO_2/SiC interface. The electric field near the SiO_2/SiC interface can be controlled by adjusting W_{jch}. In Fig. 1.15, the electric field profile in the JFET region is plotted as a function of the distance from SiO_2/SiC interface for different W_{jch} values for ACCUFETs on different starting materials. In Fig. 1.15(a), the electric field profiles are presented for an ACCUFET on a 10 μm epilayer, at a drain bias (2000 V) which is close to the breakdown voltage. It can be seen that for a small W_{jch} value of 1.5 μm, the electric field in SiC at the SiO_2/SiC interface is 0.4 MV/cm, which is much less than the peak electric field of 2.6 MV/cm in the device which occurs at a depth of about 2 μm into the JFET region of the device. The electric field at the interface increases with increase in W_{jch} and approaches the value in the bulk, because of a lower potential barriers in the wider JFET regions. The electric field in SiO_2 is about 2.5 times larger than the field in SiC at the interface because of the lower dielectric constant of







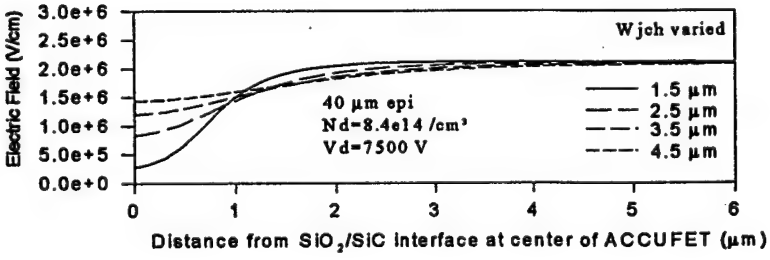


Fig. 1.15 Electric field profile in SiC as a function of the distance of from SiO_2/SiC interface at the center of the ACCUFET cell for different JFET widths for different starting materials.

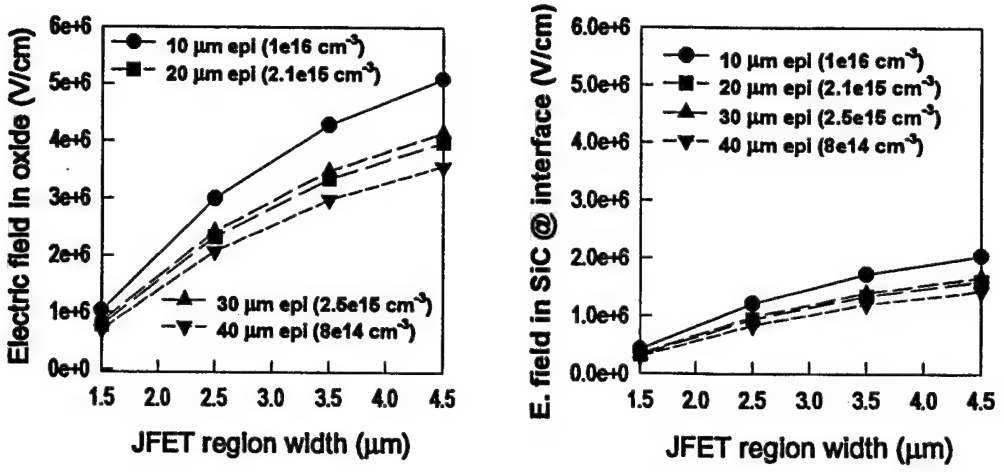
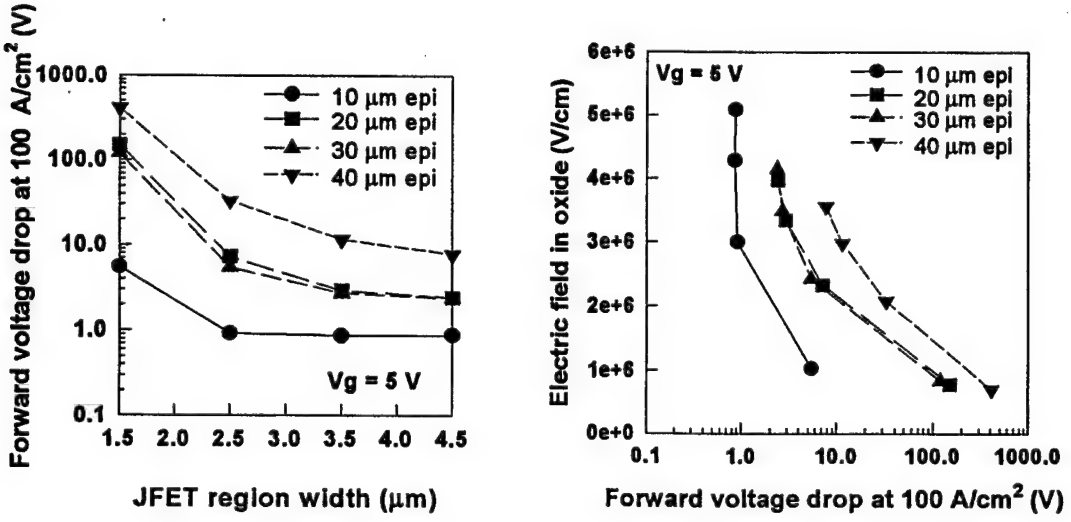


Fig. 1.16 Electric fields in SiO_2 and in SiC at the SiO_2/SiC interface as a function of JFET region width for different epilayers, when the applied drain bias is near breakdown voltage.



(a) (b)

Fig. 1.17 (a) Variation of forward voltage drop with JFET region width for different epilayers at a gate bias of 5 V. (b) Trade-off between the electric field in the oxide at device breakdown and the forward voltage drop at 100 A/cm^2 at a gate bias of 5 V.

SiO_2. This relationship is defined by Gauss' Law, which relates the electric fields in at two materials at a heterojunction:

$$\varepsilon_{ox}E_{ox} = \varepsilon_{SiC}E_{SiC} \quad (1.38)$$

where, ε and E are the dielectric constants and the electric fields in the two materials, respectively.

In Fig. 1.16, the electric fields in SiO_2 and in SiC at the SiO_2/SiC interface are plotted as a function of JFET region width for different epilayers, when the applied drain voltages are near the respective breakdown voltages. Hence, the drain voltages for the 10 μm, 20 μm, 30 μm and 40 μm thick epilayers were 2000 V, 4000 V, 5500 V and 7500 V, respectively. As noted above, the electric field in the oxide for the 10 μm epilayer increased from 1 MV/cm at W_{jch} = 1.5 μm to 5 MV/cm at W_{jch} = 1.5 μm, which is much less than the oxide breakdown strength of 10 MV/cm. In the materials of lower doping, the electric fields in SiC are lower. This results in the lower oxide electric fields observed in thicker epilayers, which have lower doping. The electric fields in SiC at the interface follow the same trends as the oxide electric fields as predicted by Gauss' Law.

1.3.1.2 Trade-off with forward voltage drop

Although reducing W_{jch} provides the advantage of low oxide electric fields, it comes with a price. When W_{jch} is decreased, the cross sectional area for current flow from the channel into the drift region decreases and this results in an increase in the resistance for the current flow through the JFET region, as discussed in section 1.2.1.3. Hence, the forward voltage drop of the ACCUFET increases with a reduction in W_{jch}. In Fig. 1.17(a), the forward voltage drop at a current density of 100 A/cm^2 is plotted as a function of W_{jch} for different epilayers, at a gate bias of 5 V. For a W_{jch} value of 1.5 μm, the forward voltage drop is about an order of magnitude higher than that for the higher values of W_{jch}. This is because the JFET region is completely pinched off at this low value of W_{jch} in all the low doped epilayers, except the 10 μm epilayer in which the doping is much higher (10^{16} cm^{-3}). As discussed in section 1.2.1.4, when the JFET region is pinched off the electrons flow by injection across a potential barrier that significantly increases the resistance. Even in the case of the 10 μm epilayer, where the forward voltage drop is orders of magnitude lower than the other cases, the width of the undepleted JFET region is very low resulting in a high JFET region resistance. Further, the forward voltage drop is higher for thicker epilayers.

At larger values of the JFET widths, the higher voltage drops in ACCUFETs on lower doped (thicker epilayer) materials are due to an increase in both the JFET as well as the drift region resistances. The JFET resistance increases in the low doped epilayers due to a reduction in the width of the undepleted JFET region through which the current flows. The drift region resistance increases due to an increase in epilayer thickness as well as a reduction in the epilayer doping. The trade-off between the electric field in the oxide at device breakdown and the forward voltage drop at 100 A/cm^2 at a gate bias of 5 V, presented in Fig. 1.17(b). It can be seen that for W_{jch} greater than 3.5 μm, the forward voltage drop does not reduce significantly. The oxide electric field for this value of W_{jch} is also well below the oxide breakdown field. Hence, the optimal value of W_{jch} was chosen to be 3.5 μm, and was used to define a typical cell for subsequent simulations.

1.3.2 Current density-Voltage (J-V) Characteristics

1.3.2.1 Effect of JFET width

The J-V characteristics of ACCUFETs on the different epilayers for different values of buried JFET width (W_{jch}) at a gate bias of 5 V are presented in Fig. 1.18. The channel length is 2.25 μm. For each of the epilayers, the J-V curves exhibit a relatively flat saturation region over a large voltage range, with saturation current densities of the order of 300 A/cm^2. The breakdown voltage and the saturation current density values are independent of W_{jch}.

The J-V characteristics, plotted over a smaller drain voltage range, are presented in Fig. 1.19. The slopes of the curves in the linear region increase with increase in W_{jch}, due to reduction in the on-resistance, as discussed in the previous section. Further, note that the J-V curves of the different epilayers (except the 10 μm epilayer) at Wjch = 1.5 μm exhibit noticeable current only at large drain voltages. The offset drain voltages at which any noticeable current is observed, increase with reduction in the doping of the epilayer. These are observed to be 0 V, 32 V, 44 V and 140V in epilayers with doping $1x10^{16}$ cm^{-3}, $2.5x10^{15}$ cm^{-3}, $2.1x10^{15}$ cm^{-3}, and $8.4x10^{14}$ cm^{-3}, respectively. The offset voltage is observed because the JFET width is completely pinched-off by the depletion from the buried p-n junction, and current transport occurs by injection over a potential barrier. Hence, the JFET region in the device exhibits triodelike behavior, discussed in section 1.2.1.1. In fact, a closer look at these curves reveals that the current increases exponentially just after the offset voltage as observed in the triodelike behavior. Then, it exhibits MOSFET-like behavior by increasing linearly and saturating at the expected saturation current values. Note that the offset voltage in the highly doped epilayer is zero, because the JFET width, in this case, is not completely pinched-off due to a narrower depletion spread from the buried p-n junction. However, the resistance of this device is still much higher than that at the higher W_{jch} values, because of a much narrower undepleted width for the current to flow through. Also note that, for the lowest doping material, a small voltage offset of 2 V is observed even when the JFET width is increased to 2.5 μm. These observations show that optimizing the parasitic JFET region is a critical to the design of high voltage ACCUFETs.

1.3.2.2 Effect of channel length

The J-V characteristics of ACCUFETs on the different epilayers for different values of channel length (L_{ch}) at a gate bias of 5 V, are presented in Fig. 1.20. The width of the buried JFET region (W_{jch}) is 3.5 μm. For each of the epilayers, the J-V curves exhibit a relatively flat saturation region over a large voltage range. However, the effects of channel length modulation can be distinctly observed in the curves for the 1.25 μm channel length cases. The slopes of these curves are much larger than those for the higher values of L_{ch}. The effects of channel length modulation on the saturation current densities and the slopes of the J-V curves in the saturation region, are negligible for Lch ≥ 2.25 μm. The breakdown voltage is independent of the channel length.

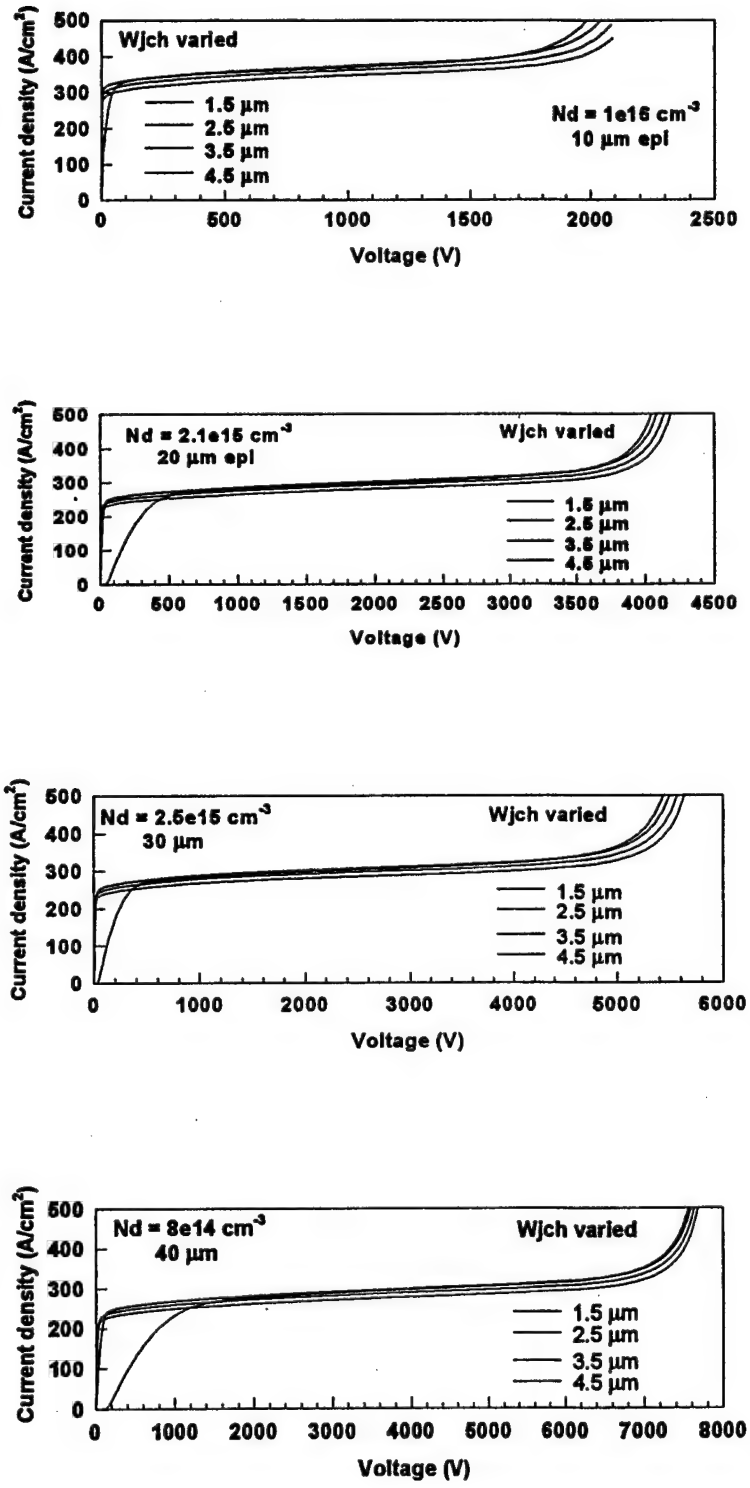


Fig. 1.18 J-V characteristics of the different epilayers at a gate bias of 5 V exhibiting breakdown voltage dependence on JFET width.

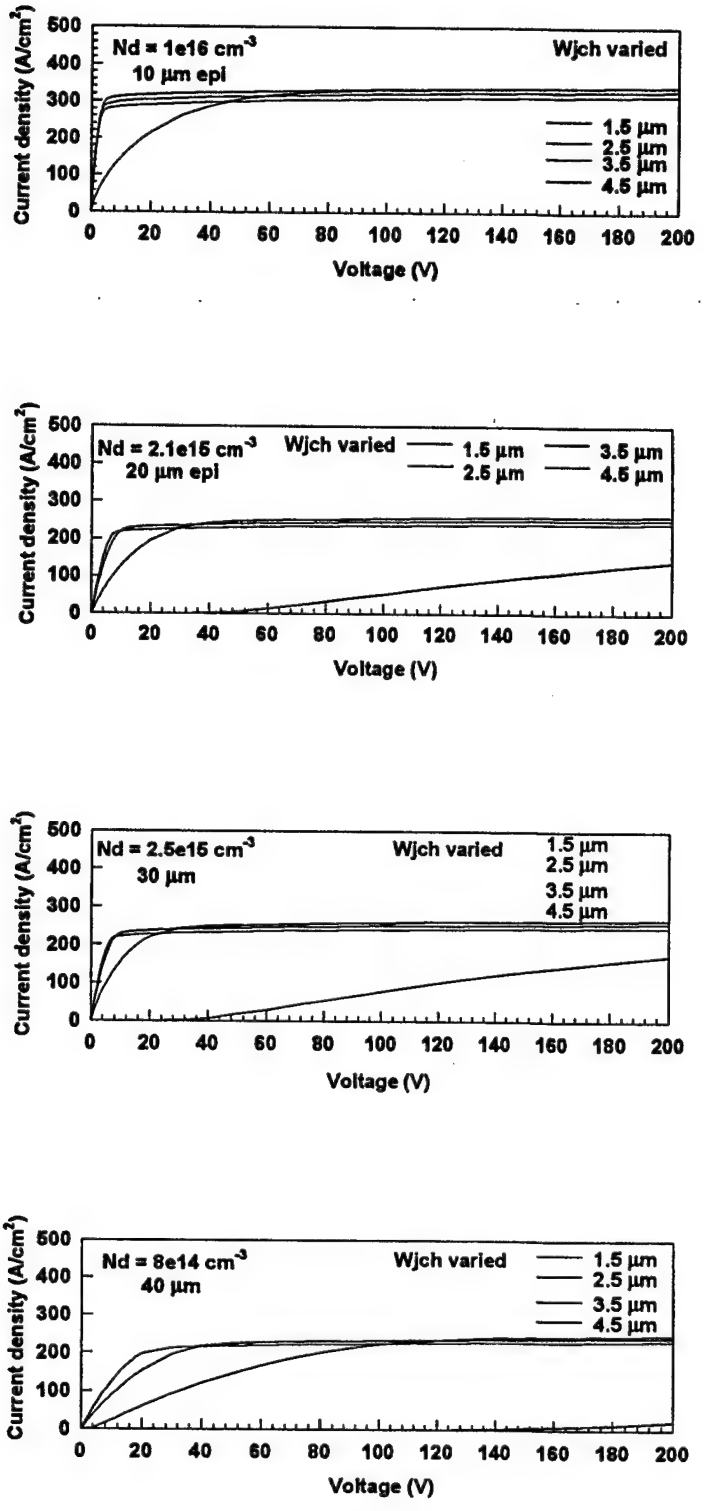


Fig. 1.19 J-V characteristics of the different epilayer materials at a gate bias of 5 V exhibiting on-resistance dependence on JFET width.

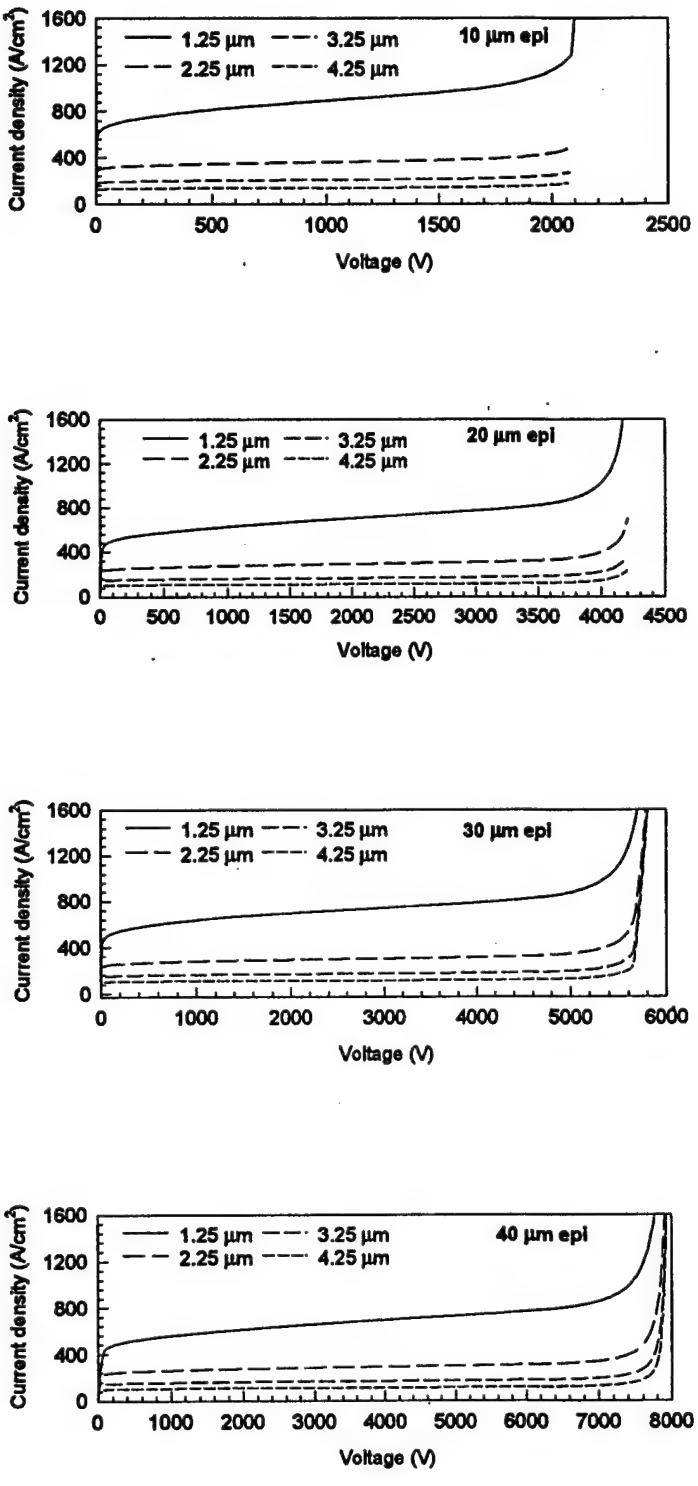


Fig. 1.20 J-V characteristics of the different epilayer materials at a gate bias of 5 V exhibiting breakdown voltage dependence on channel length.

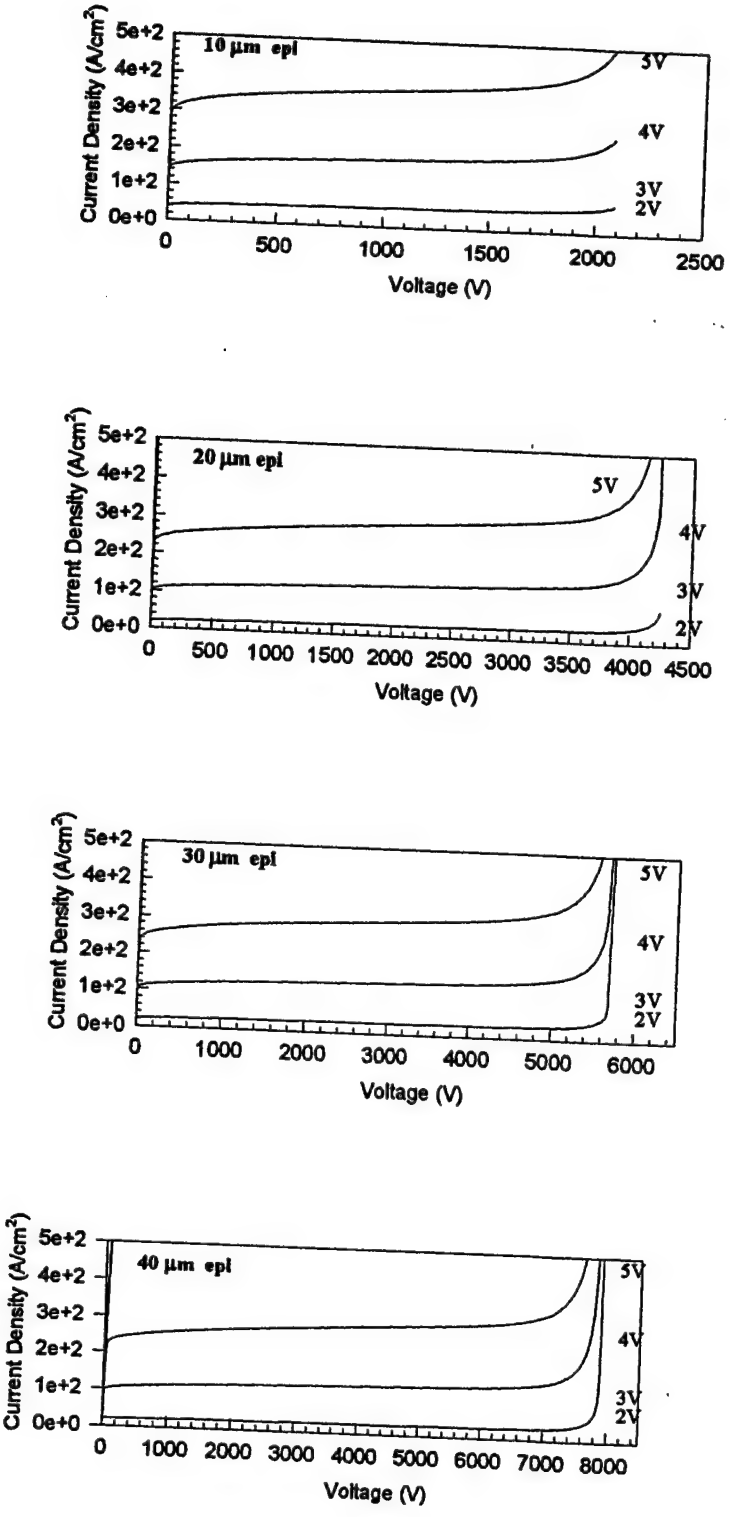


Fig. 1.21 Forward blocking safe operating area (FBSOA) of an ACCUFET on different epilayer materials.

1.3.2.3 Effect of gate bias

The J-V characteristics of ACCUFETs on the different epilayers for different values of gate bias (Vg) is presented in Fig. 1.21. W_{jch} and L_{ch} are 3.5 μm and 2.25 μm, respectively. For each of the epilayers, the J-V curves exhibit a relatively flat saturation region over a large drain voltage range. The saturation current densities decrease with decreasing values of epilayer doping, which is the case with the different materials, as discussed in the previous section. In all cases, these devices exhibit a square forward blocking safe operating area (FBSOA).

1.4 ACCUFET On-Resistance

The on-resistance of a power MOSFET is the total resistance between the source and drain terminals in the on-state. The on-resistance is an important device parameter because it determines the maximum current rating. The power dissipation in the power MOSFET during current conduction is given by

$$P_D = I_D V_D = I_D^2 R_{on} \tag{1.39}$$

Expressed in the terms of chip area A, this is

$$\frac{P_D}{A} = J_D^2 R_{on,sp} \tag{1.40}$$

where (P_D/A) is the power dissipation per unit area; J_D is the on-state current density; and $R_{on,sp}$ is the specific on-resistance. Thus, for a fixed maximum power dissipation, the maximum operating current density varies inversely with the square root of specific on-resistance.

1.4.1 Analytical model

One of the very important goals when designing a power MOSFET is to minimize its on-resistance. Hence, it is important to understand the individual components of the on-resistance so that the device can be carefully engineered to meet its application requirements. With this objective in mind, an analytical model for the on-resistance of an ACCUFET is discussed here, which will provide insights into the considerations for the design of ACCUFETs.

The total specific on-resistance of an ACCUFET is modeled to be comprised of the N+ source resistance (R_{N+}), the channel resistance (R_{ch}), the JFET region resistance (R_j), the drift region resistance (R_d) and the substrate resistance (R_{sub}), as shown in Fig. 1.22. Hence,

$$R_{on} = R_{N+} + R_{ch} + R_j + R_d + R_{sub} \tag{1.41}$$

The subscript, sp, is dropped from all specific on-resistance components for convenience. Additional resistances can arise in a real device due to poor source and drain contacts.

The source specific resistance, R_{N+}, is given by

$$R_{N+} = \frac{1}{4} \rho_{sn+} . L_{n+} . W_{cell} \tag{1.42}$$

where, ρ_{sn+} and L_{n+} are the sheet resistance and the length of the source region, respectively, and W_{cell} is the cell width.

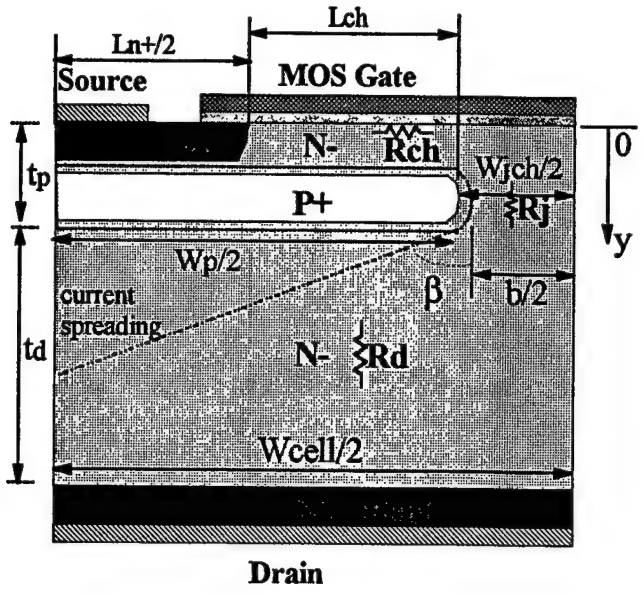


Fig. 1.22 Specific on-resistance components in an ACCUFET.

The channel specific resistance, R_{ch}, can be adapted from Eq. (1.21) and expressed for an accumulation channel as

$$R_{ch} = \frac{L_{ch} W_{cell}}{\mu_{na} C_{ox} (V_G - V_{Ta})} \tag{1.43}$$

where, L_{ch} is the channel length, μ_{na} is the accumulation channel mobility, C_{ox} is the oxide capacitance, V_G is the gate voltage, and V_{Ta} is the accumulation threshold voltage.

To derive an expression for the JFET region specific resistance, Rj, it is assumed that the electrons flowing out of the channel pass through an undepleted JFET region of width b and length t_p. The length t_p, as illustrated in Fig. 1.22, extends from the surface of SiC at the gate to the bottom of the depletion layer at the buried p-n junction. Hence, t_p is the sum of the depth of the buried p-n junction, which is approximately 1 μm based on simulations on *SUPREM*, and the width of the depletion region, W_d, as given by Eq. (1.31):

$$W_d = \sqrt{\frac{2\varepsilon_s (V_{bi})}{qN_D}} \tag{1.44}$$

where, the built-in junction potential, V_{bi}, is described by Eq. (1.32). The width of the undepleted JFET region, b, is given by

$$b = W_{jch} - 2W_d \tag{1.45}$$

Hence, the expression for JFET region specific resistance can be derived by adapting Eq. (1.9) to give

$$R_j = \frac{t_p W_{cell}}{q\mu_n n_D b} \tag{1.46}$$

where, μ_n is the c-axis mobility in the JFET region, and n_D is the majority carrier concentration in the undepleted JFET region.

The drift region specific resistance, R_d, has been derived in section 1.2.3. It is given by

$$R_d = \frac{W_{cell}}{q\mu_n n_D (2\tan\beta)} ln\left[1+\frac{2t_d \tan\beta}{b}\right]; \qquad td < \frac{(W_p+2W_d)}{2\tan\beta} \tag{1.47}$$

and,

$$R_d = \frac{W_{cell}}{q\mu_n n_D (2\tan\beta)} ln\left[1+\frac{W_p+2W_d}{b}\right] + \frac{\left(t_d - \frac{W_p+2W_d}{2\tan\beta}\right)}{q\mu_n n_D}; \qquad td > \frac{(W_p+2W_d)}{2\tan\beta} \tag{1.48}$$

where, W_p is the width of the buried P+ layer, and t_d is the thickness of the drift region which the difference of the epilayer thickness and t_p. β is the angle of current spreading in the drift region.

The substrate specific resistance, R_{sub}, is given by

$$R_{sub} = \frac{\rho_{sub} t_{sub}}{n_{cs}} \tag{1.49}$$

where, t_{sub} is the substrate thickness, ρ_{sub} is the resistivity of the substrate, and n_{cs} is a factor that accounts for the current spreading in the substrate. It must be noted that while determining the device specific resistance and in simulations, the current can flow only within the cell, in which case, $n_{cs} = 1$. However, when small devices are made on a large wafer, the current flowing out from the device spreads in the substrate resulting in a much smaller resistance contribution from the substrate than that calculated using above equation.

In all the above described equations, the majority carrier (electron) concentration n_D in a non-degenerate semiconductor can be evaluated [5] using the following

$$n_D = \frac{N_D}{1+\frac{g_n n_D}{N_C} exp\left(\frac{\Delta E}{kT}\right)} \tag{1.50}$$

where, N_D is the doping concentration, g_n is the degeneracy factor, N_C is the effective density of states in the conduction band, and ΔE is the ionization energy. N_C is proportional to $T^{1.5}$.

In real devices, it is also important to include the effect of a finite contact resistance. This is particularly relevant because the area of the contact to source region is a small fraction of the total cell area. This tends to amplify the contact resistance contribution. This does not occur on the drain side because the contact covers the entire surface of the back. Thus, the drain contact resistance contribution to the specific resistance is given by

$$R_{CD} = \rho_c \tag{1.50}$$

where, ρ_c is the specific contact resistance in Ωcm^2. Similarly, if the contact area of the metal to the N+ source is A_{CS}, the contribution to the specific resistance by the source contact is given by

$$Rcs = \frac{A_{cell}}{Acs}\rho_c \tag{1.51}$$

1.4.2 Simulation results

The important material and device parameters used in simulations of output characteristics of 4H-SiC ACCUFET that were required for the calculation of the specific on-resistance components are shown in Fig. 1.23. The ACCUFET structure used for this purpose had a cell width (W_{cell}) of 10 μm, a JFET width (W_{jch}) of 3.5 μm and a channel length (L_{ch}) of 2.25 μm. The substrate thickness used in the simulations was 2 μm. The epilayer and substrate doping were based on the actual starting material for the fabrication of the devices. The mobility and the threshold voltage values were extracted from the simulations. The undepleted JFET width (b) and the thickness of the JFET region (t_p), used in the analytical model for on-resistance, were obtained from the plots for depletion and current flowlines for the ACCUFETs at a drain bias of 0.1 V (Fig. 1.24). To evaluate the spreading angle, β, the current distribution in the drift region was recorded at different depths. It was observed that the current flows uniformly beyond a depth of 15 μm. Based on this observation, the spreading angle was calculated as follows

$$\tan\beta = \frac{\frac{W_{cell}}{2} - \frac{b}{2}}{15 - t_p} \tag{1.52}$$

where, all the dimensions are in microns.

Epi thickness (μm)	10	20	30	40
Epi doping (1/cm3)	1e16	2.1e15	2.5e15	8.4e14
Substrate thickness (μm)	2.0	2.0	2.0	2.0
Substrate doping (1/cm3)	1e19	6e18	7.8e18	8.6e18
Channel mobility (V/cm².s)	260	260	260	260
Drift mobility (V/cm².s)	813	891	885	913
Substrate mobility (V/cm².s)	75	105	90	80
Threshold voltage (V)	1.97	2.21	2.23	2.26
Undepl. JFET width, b (μm)	2.0	1.3	1.4	0.6
JFET region thick., tp (μm)	1.45	2.1	2.0	2.8
tan(β)	0.66	0.72	0.71	0.79

Fig. 1.23 Material and device parameters used for simulations on 4H-SiC ACCUFETs. (JFET width = 3.5 μm, Channel length = 2.25 μm, Gate oxide thickness = 500 Å and Gate bias = 5V)

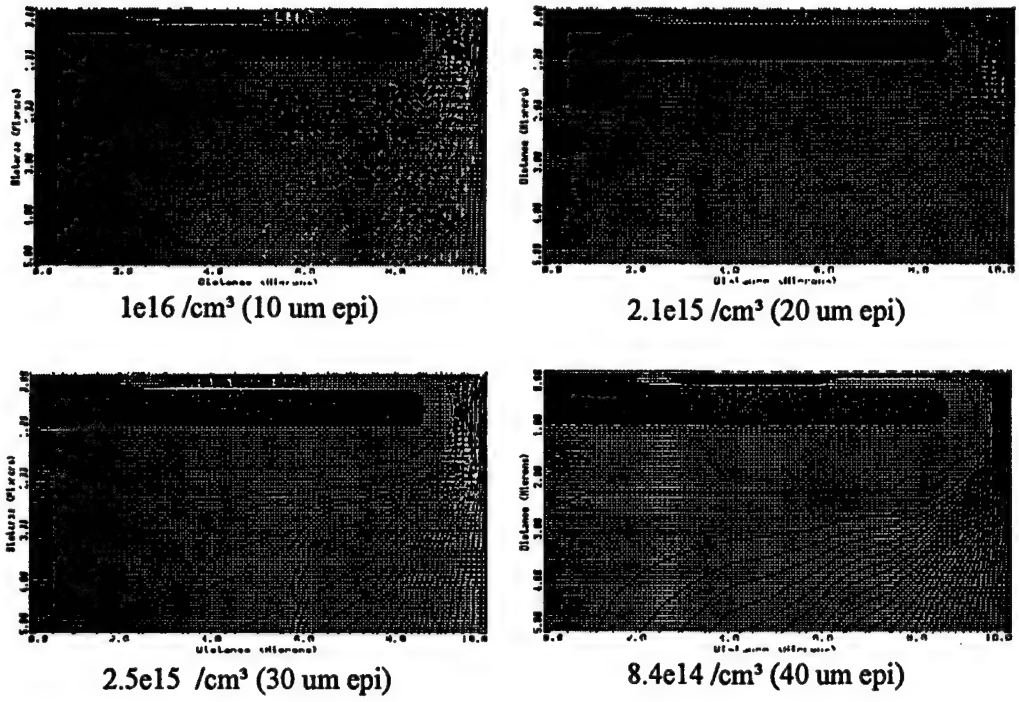


Fig. 1.24 Current flowlines in 4H-SiC ACCUFETs on epilayers of different doping densities at a drain bias of 0.1 V.

Using these parameters and the equations discussed in the previous section, the individual specific on-resistance components were evaluated for different epilayers as listed in Fig. 1.25. Note that the total specific on-resistance values calculated using the model compare well with those obtained from simulations.

The channel and the drift region resistance are found to contribute significantly to the on-resistance. The channel resistance is most dominant in the ACCUFET on the 10 μm epilayer (device 1), which has the highest doping of $1x10^{16}$ cm^{-3}. The high doping in this epilayer results in very low JFET and drift region resistance values. However, as the epilayer doping is reduced, the contributions from the JFET and the drift regions increase, and the channel resistance is no longer the dominant resistance, as observed in the case of the 40 μm epilayer (device 4) which has the lowest doping of $8.4x10^{14}$ cm^{-3}. In fact, the contribution of the channel resistance to the total on-resistance reduces from 71 % in device 1 to only 9 % in device 1.

In contrast, the contribution of the JFET region to the total on-resistance increases from only 7 % in device 1 to about 30 % in device 1. This indicates that the ACCUFET structure used in this simulation is not optimized for the low doping levels. The ACCUFETs on epilayers with low doping densities need to be designed differently from those with high doping densities. The JFET region resistance of the ACCUFETs on low doping epilayers can be reduced substantially by increasing the width of the JFET region and/or by increasing the doping in the JFET region.

Epi Thickness (μm)	10	20	30	40
Rn+source (mΩ.cm²)	0.28	0.28	0.28	0.28
Rchannel (mΩ.cm²)	8.22	8.22	8.22	8.22
Rjfet (mΩ.cm²)	0.77	5.14	4.04	26.53
Rdrift (mΩ.cm²)	2.28	14.24	14.71	54.89
Rsubstrate (mΩ.cm²)	1.67e-3	1.98e-3	1.78e-3	1.82e-3
Rtotal (mΩ.cm²)	**11.5**	**27.9**	**27.2**	**89.8**
Rtotal (simulatn.)	7.1	23.6	23.9	98
PunchThru (PT) parallel plane Rdrift	0.77	6.7	8.5	32.6
Rtotal (simulatn.)/ PT parallel plane Rdrift	9.2	3.5	2.8	3.0

Fig. 1.25 Specific on-resistance components in ACCUFETs on 4H-SiC with material and device parameters as described in Fig. 1.23. (JFET width = 3.5 μm, Channel length = 2.25 μm, and Gate bias = 5V)

The contribution of the drift region to the on-resistance also increases substantially from device 1 to device 4, due to an increase in the epilayer thickness and a reduction in the epilayer doping. The contribution increases from 20 % in device 1 to 61% in device 1. As discussed earlier, the current flow into the drift region can be categorized into two regions: one in which the current spreads and the other in which the current flows uniformly. The specific resistance of the region in which the current spreads is much higher than in the region of uniform current flow. Hence, to minimize the drift region resistance, it is important to minimize the contribution of the spreading resistance, which is a function of the epilayer thickness, the width of the buried P+ finger, the cell width (which also depends on the buried P+ layer), and the spreading angle. The spreading angle, which is a material parameter, is shown, by simulations, to reduce by 14% with the increase in epilayer doping between device 4 and device1. However, the contribution of the spreading resistance term to the drift region resistance is influenced most by the ratio of the epilayer thickness to the cell width. This ratio needs to be as large as possible to minimize the contribution of the spreading resistance. The cell width can be reduced considerably by designing the ACCUFET with sub-micron design rules. In the present designs, sub-micron design rules could not be used because the available stepper which can pattern sub-micron features is not configured to handle the small (1.375 inch diameter) silicon carbide wafers. For the ACCUFET under consideration, the drift region resistance can be compared with the punch-through parallel plane resistance. The latter is defined as the resistance of the drift region when the current flows uniformly through the entire drift region. The ratio of the total drift region resistance to the punch-through parallel plane resistance reduces from 2.96 in device 1 to 1.68 in device 1. This corresponds to an increase in the epilayer thickness to cell width ratio from 0.5 in device1 to 2.0 in device 1. Thus, in the drift region, the current spreading from the relatively narrow JFET region

helps in reducing the resistance of the device, but it is desirable that the current spreads quickly and flows uniformly through the drift region.

The calculated substrate specific resistance (~$2x10^{-3}$ $m\Omega.cm^2$) is extremely low in the simulations because of a small substrate thickness. In real devices, the substrate thickness is about 300 μm. The substrate resistance contribution is given by Eq. (1.49) using n_{cs} = 1. The calculated R_{sub} for the 300 μm thick substrate is 0.4 $m\Omega.cm^2$. However, the contribution of the substrate resistance in the measured devices was very small due to current spreading in the substrate. Simulations of the current flow from the small active area of the fabricated devices through the substrate have shown that the actual resistance of the substrate is about 10X lower than that calculated by assuming uniform current flow through the substrate, because of the current spreading.

For each of the epilayers, the on-resistance of the device is also compared with the punch-through parallel plane drift region on-resistance. This ratio is of the order of only 3X for epilayers of thickness ≥ 20 μm. For the 10 μm epilayer, the ratio is about 9X. As discussed earlier, this is because of the dominance of the channel resistance in the ACCUFET on the 10 μm epilayer, and that of the drift region resistance in the ACCUFET on the 40 μm epilayer.

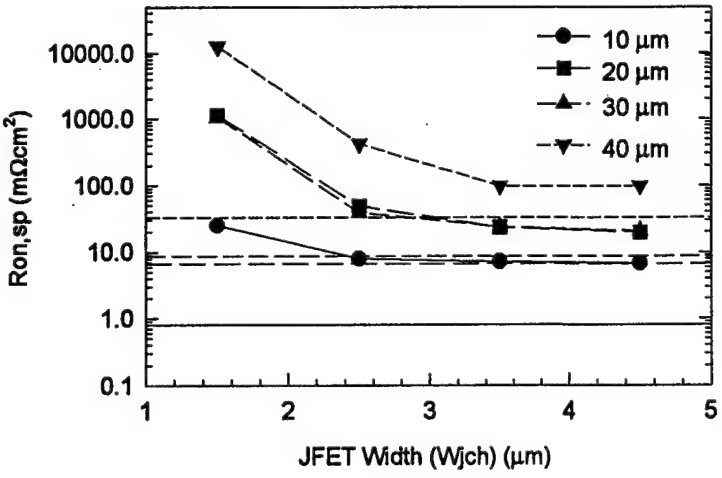


Fig. 1.26 Dependence of specific on-resistance on JFET width in different epilayer materials. The horizontal straight lines indicate the punch-through parallel-plane drift region specific resistance for each case. (Channel length = 2.25 μm, Gate bias = 5V)

1.4.3 Effect of JFET width

The dependence of specific on-resistance on JFET width (W_{jch}) in different epilayers is shown in Fig. 1.26. It also shows horizontal straight lines which represent the punch-through parallel plane drift region specific resistance for each case. For these simulations, the channel length was 2.25 μm and the gate bias was 5V. The specific on-

resistance is observed to reduce rapidly with increase in Wjch, but does not change much for Wjch > 3.5 μm.

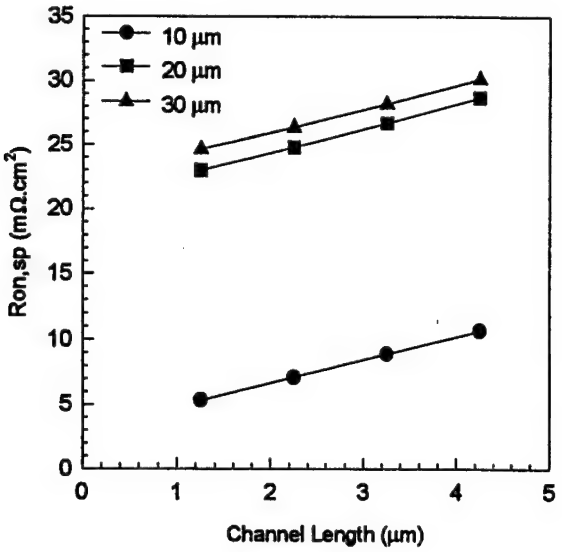


Fig. 1.27 Dependence of specific on-resistance on channel length in different epilayer materials. (JFET width = 3.5 μm, Gate bias = 5 V)

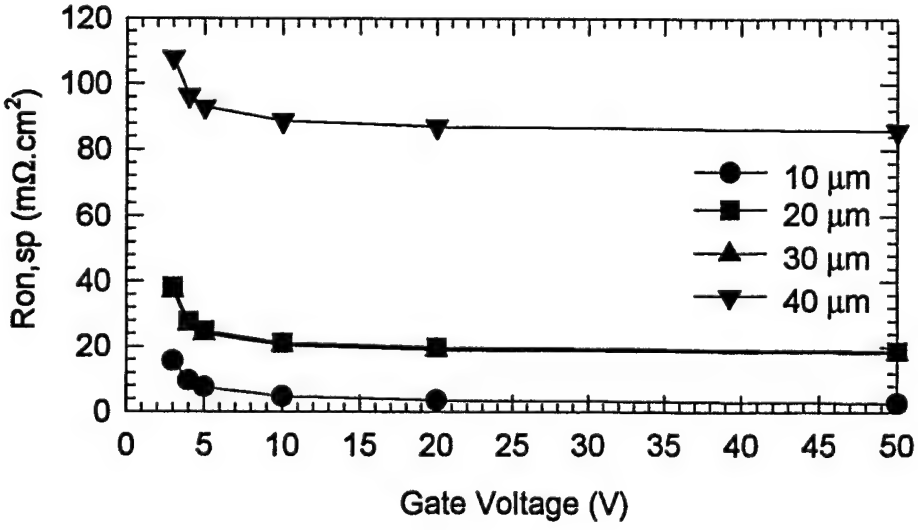


Fig. 1.28 Dependence of specific on-resistance on gate bias in different epilayer materials. (JFET width = 3.5 μm, Channel length = 2.25 μm)

Fabrication of High Voltage 4H-SiC ACCUFETs

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Abstract

A new process for fabrication of high voltage 4H-SiC ACCUFETs has been designed using insights gained from studying previously fabricated ACCUFETs. The device designs and the process flow for the fabrication of the high voltage planar ACCUFETs in 4H-SiC are presented in detail. Further, the process-induced variations of the key design parameters of an ACCUFET are discussed. The fabrication of devices such as the Junction Barrier Schottky (JBS) diodes and the Junction Field Effect Transistors (JFET) is totally compatible with this process without the use of any additional mask levels or process steps.

1.1 Introduction

The ACCUFET had previously been demonstrated at PSRC on both 6H-SiC and 4H-SiC on 10 μm thick epilayers [1]. While the ACCUFETs on 6H-SiC exhibited excellent electrical characteristics, those on 4H-SiC performed poorly. Hence, several test runs and measurements were performed to understand how to improve the specific on-resistance and the breakdown voltage of these devices. The insights thus gained resulted in several changes in the process flow as well as the device design for fabrication of improved high-performance 4H-SiC high voltage ACCUFETs. The new process for fabrication of ACCUFETs was designed using these changes. The fabrication of devices such as the Junction Barrier Schottky (JBS) diodes and the Junction Field Effect Transistors (JFET) is totally compatible with this process without the use of any additional mask levels or process steps. Here, the device designs and the process flow for the fabrication of the high voltage planar ACCUFETs in 4H-SiC are discussed in detail.

Mask Level	Mask Name	Mask Type	Photoresist	Alignment to (level)
1	Align Mark	DF	Positive	-
2	P+ Buried	DF	Positive	1
3	P+ Sinker	DF	Positive	2,1
4	N+ Source	DF	Positive	2,1
5	Poly	LF	Positive	1,4,2
6	Contact	DF	Positive	5,4,1
7	Aluminum	LF	Negative	6
8	Titanium	LF	Negative	6
9	Nickel	LF	Negative	6
10	Edge Term.	LF	Positive	9

DF = Dark field
LF = Light field

Fig. 1.1 Mask levels used for the ACCUFET process run.

1.2 Process Sequence

A 10 mask process was defined to fabricate the high voltage planar ACCUFETs. The process parameters were determined by process simulations using *SUPREM III* as well as by test runs. The mask names and the mask types (dark field or light field) are listed in Fig. 1.1. Fig. 1.1 also summarizes the type of photoresist (positive or negative) used with each mask level, and the levels matched while drawing alignment patterns on the layout. The alignment scheme for the 10 mask levels is shown graphically in Fig. 1.2. The starting wafers for 4H-SiC were single crystal N-type ($3x10^{18}$ cm^{-3}) substrates with 10, 20, 30 and 40 μm thick nitrogen doped epilayers with different as listed in Fig. 1.3. The salient features of the process flow are compiled in Fig. 1.4. All wafers were initially cleaned using a five minute dip in a JT Baker clean solution. The first mask level was designed for creating alignment marks on the SiC wafers. The alignment marks were etched into SiC by reactive ion etching (RIE) using photoresist as the mask. The

following procedure was used. After the JT Baker clean, all wafers were dried on a hot plate at 115 °C for 5 minutes. Next, hexamethyldisilazane (HMDS) and then, the photoresist (JSR 10 cp) were spun on the wafers, each at a speed of 4500 rotations per minute and for 40 seconds. These wafers were baked (pre-expose bake) at 90 °C for 1 minute. Then, the wafers were exposed using the first mask level on the Karl Suss MJB3 contact printer at an intensity of 15 mW/cm^2 for 25 seconds in a constant power mode. After a post-exposure bake at 115 °C for 1 minute, the patterns were developed using a 1 minute dip in the developer solution. A post-develop bake at 90 °C was done for 1 minute to reduce the moisture content on the wafers. The RIE was performed using the Oxford Plasmalab 90 system. SiC was etched using a mixture of sulfur hexaflouride (SF_6) at 9 sccm and oxygen (O_2) at 1 sccm for 8 minutes at a power of 120 W, a pressure of 50 mTorr and a temperature of 15 °C. This resulted in SiC alignment marks that were approximately 0.25-0.3 μm deep. After RIE, the photoresist (PR) was stripped from the wafers using a 5 minute dip in the Nanostrip solution. Any remnants of PR were removed using a room temperature oxygen plasma in an Asher by March Instruments at 300 W and 600mTorr at an oxygen flow of 80 sccm. Then, the wafers were cleaned using JT Baker clean solution.

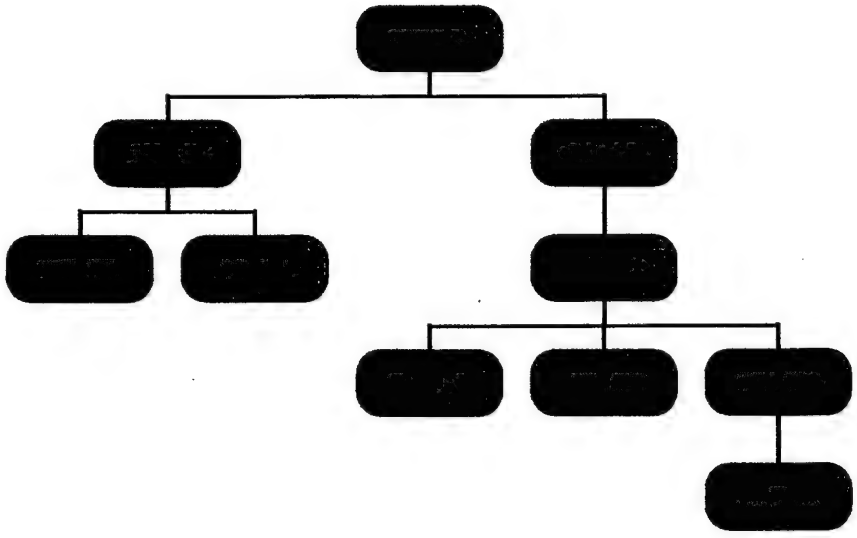


Fig. 1.2 Mask alignment scheme.

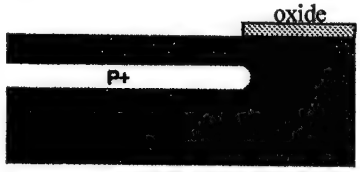
The second mask level was used for creating the buried P+ layer on the wafers. The buried junction was formed by boron implantation using a 1.6 μm thick deposited silicon dioxide as the mask. This thick oxide was deposited using plasma enhanced chemical vapor deposition (PECVD) in an Oxford Plasmalab 90 system. The process recipe deposited the oxide for 75 minutes using nitrous oxide (N_2O) at 710 sccm and a 2% mixture of silane (SiH_4) in helium (He) at 170 sccm, at a power of 20 W, a pressure of 1 Torr, and a substrate temperature of 300 °C. The SiC wafers were loaded at room temperature into the PECVD chamber to reduce thermal stress on the wafers. After oxide deposition, the second level mask was used to pattern PR on the wafers using the standard

Wafer Number	Epilayer Thickness (μm)	Epilayer Doping ($1/cm^3$)	Substrate Thickness (inches)	Substrate Doping ($1/cm^3$)
1	10	1e16	0.0146	1e19
2	10	1e16	0.0132	1e19
3	20	1.5e15	0.0104	8.6e18
4	20	2.1e15	0.0113	6e18
5	30	2e15	0.0151	6.5e18
6	30	2.5e15	0.0121	7.8e18
7	40	2e15	0.0170	6.5e18
8	40	8.6e14	0.0138	8.6e18

Fig. 1.3 Specifications for starting 4H-SiC wafers.

Mask 1 ***Etch alignment marks into RCA-cleaned SiC wafers using SF_6/O_2 Reactive Ion Etching (RIE).***

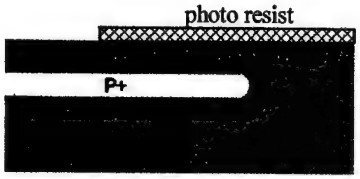
Mask 2



Buried P implant: Boron , 380 KeV, 1E14 /cm², 1000 °C, 0°.

Mask 3 ***P+ sinker implant: Aluminum, 25 KeV, 4E15/cm²; 75 KeV, 1e15/cm²; 200 KeV, 1E14/cm², 1000 °C, 0°.***

Mask 4

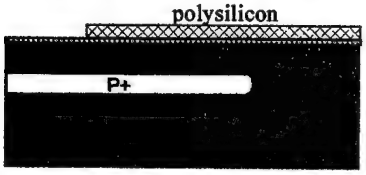


N+ source implant: Nitrogen, 40, 100 KeV, 8E14/cm², R.T, 0°. Implant back of the wafer also.

Wet blanket etch of oxide
Implant anneal: 1500°C, 30 min, Argon

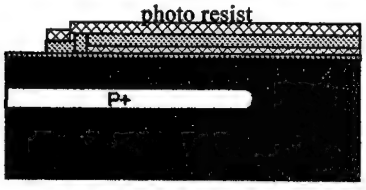
Gate oxidation:
- ***Thermal : 1100 C, wet, 120 min, Reoxdn at 950 C, wet, 60 min***
- ***LPCVD (LTO) : 410 C, 750 mTorr***

Mask 5



Polysilicon: LPCVD, 0.5um, P doped at 900 C, 60 min.
Pattern using RIE
Poly-oxidation:10/20/10 D/W/D

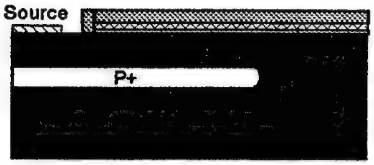
Mask 6



Field oxide : LPCVD, 0.5 um
Contact etch: RIE, contacts to both poly as well as the metals

Mask 7 ***Aluminum metallization to contact P+ : 2000A Al; Pattern using lift-off technique; Post metallization anneal at 700 °C***

Mask 8



Titanium metallization to contact N+ and Aluminum: 2000A/ 2000A Ti/Al; Same on backside; Pattern using lift-off technique; Post metallization anneal at 500 C.

Mask 9 ***Nickel metallization for edge termination : 500A/2000A Ni/Al; Pattern using lift-off technique; Post metallization anneal***

Mask 10 ***Argon implants for edge termination : 30 KeV, 2e15/cm², RT.***

Fig. 1.4 Process flow diagram for ACCUFET fabrication.

procedure as described in the previous paragraph. However, in this case, HMDS and PR were spun at an rpm of 3500 resulting in a 1 μm thick PR on the wafers. Next, to open windows for the high energy boron implants, approximately 1.3-1.4 μm of the 1.6 μm thick oxide was etched by RIE using PR as the masking material, and the remaining oxide was removed by a dip in a buffered oxide etch (BOE) solution. RIE of the oxide was done using a mixture of triflouromethane (CHF_3) at 25 sccm and Argon (Ar) at 25 sccm for 45 minutes at a power of 100 W, a pressure of 60 mTorr and a temperature of 20 °C. After stripping the PR, the wafers were sent to Implant Sciences for boron implants at 1000 °C at an energy of 380 keV, a dose of $1x10^{14}$ cm^{-2} and a 0° tilt angle. The dose and the energy values for obtaining the buried P+ layer were determined by ion-implantation simulations.

The third mask level was used for creating the P+ sinker layer on the wafers for making contact to the buried P+ layer. The sinker layer was formed by aluminum implantation using a 1 μm thick deposited silicon dioxide as the mask. This thick oxide was also deposited by PECVD in an Oxford Plasmalab 90 system for 51 minutes using the same recipe as described in the previous paragraph. After oxide deposition, the third level mask was used to pattern PR on the wafers using the standard procedure as described in the previous paragraph. Next, to open windows for the high energy boron implants, most of the thick oxide was etched by RIE using the above-mentioned recipe for 30 minutes with PR as the masking material, and the remaining oxide was removed by a dip in a buffered oxide etch (BOE) solution. After stripping the PR, a 300 ❶ thick pad oxide was deposited in 1.5 minutes using PECVD. The pad oxide ensured a high doping concentration at the SiC surface, which is desirable for minimizing contact resistance. The wafers were sent to Implant Sciences for multiple low energy aluminum implants done at 1000 °C at energy and dose combinations of 25 keV, $4x10^{15}$ cm^{-2}; 75 keV, $1x10^{15}$ cm^{-2}; and 250 keV, $8x10^{14}$ cm^{-2}; and a 0° tilt angle.

The fourth mask level was used for creating the N+ source layer on the wafers. The N+ source layer was formed by nitrogen implantation using photoresist as the mask.

After aluminum implants, approximately 1 μm of oxide was etched using BOE to open windows within which the nitrogen implants could be made. Next, a 800 ❹ thick pad oxide was deposited in 4 minutes using PECVD. After oxide deposition, the fourth level mask was used to pattern PR on the wafers using the standard procedure as before. However, in this case, the post-develop bake was done at 115 °C for 5 minutes to densify the PR. The wafers were sent to Implant Sciences for multiple low energy nitrogen implants at room temperature at energy and dose combinations of 40 keV, $8x10^{14}$ cm^{-2} and 100 keV, $8x10^{14}$ cm^{-2}, and a 0° tilt angle.

After the implants, the PR was stripped and the oxide was removed with a blanket etch using BOE. The wafers were then cleaned using a standard RCA clean. The implants were given a high temperature (1500 °C) proximity-anneal for 30 minutes in a SiC crucible in an Argon ambient. The proximity anneal is done by capping the process wafer with another silicon carbide wafer, and placing both in a silicon carbide crucible. This is done to provide sufficient silicon carbide over-pressure to prevent the formation of pits by decomposition of silicon carbide at high temperatures. For the anneal, the furnace was ramped up at 5 °C/min from a standby temperature of 800 °C to 1500 °C, and then, ramped down at 3 °C/min in an Ar ambient. The anneal temperature of 1500 °C was used instead of the proposed value of 1600 °C because of process difficulties encountered at the higher temperature. It was observed that the test SiC samples annealed at 1600 °C exhibited oxidation as well as surface damage in the form of pits, which was attributed to the degradation in the quality of the silicon carbide crucible.

Next, a thin layer of sacrificial oxide was thermally grown on all wafers. For thermal oxidation, the wafers were placed horizontally on a quartz boat and loaded into the high temperature furnace at 800 °C. The wafers were heated to 1100 °C at 5 °C /min in an oxygen ambient. Then, the oxide was grown for 60 minutes by exposure to nitrogen bubbled through DI water at 95 °C. The wafers were cooled to 800 °C at 3 °C/min in dry nitrogen. This oxide layer was completely removed by buffered oxide etch (BOE).

After the sacrificial oxidation on the wafers, a process split was introduced to fabricate thermally grown as well as deposited gate oxide. Of the eight silicon carbide wafers, on wafers 1, 3 5 and 7, the gate oxide was deposited by Low Pressure Chemical Vapor Deposition (LPCVD) using disilane and oxygen at 410 °C and 750 mTorr. The wafers were placed vertically on a silicon carbide boat during deposition, which was done for 8 minutes. The resultant oxide films were extremely non-uniform in thickness. The thickness variation was found to be as high as 150 ❹ between the top and the bottom of the wafer in some of the wafers, with the thicker film at the top, but was fairly uniform from left to right. To improve the breakdown strength of the oxide and to reduce the fixed oxide charge and the density of the interface states, the deposited oxide was subjected to the following thermal cycles in the high temperature furnace[2]. The wafers with the oxide were loaded on a quartz boat into the furnace at 800 °C. The furnace temperature was ramped up to 1250 °C at 5 °C/min with Argon in the wafer ambient and was maintained at that temperature for 60 minutes. The temperature was then ramped down at 3 °C/min to 1100 °C with Oxygen as the ambient gas. At 1100 °C, the wafers were exposed to wet nitrogen (bubbled through DI water at 95 °C) for 60 minutes, which was followed by an anneal in Argon for 60 minutes. After ramping the temperature down at 3 °C/min in an Argon ambient, the wafers were re-oxidized at 950 °C in wet nitrogen

for 60 minutes. Finally, the wafers were cooled to 800 °C in dry nitrogen at 3 °C/min. This treatment increased the gate oxide thickness by about 150 ❹. The thickness variation of the resultant oxide films is shown in Fig. 1.5. It is important to note this variation for the device analysis because both the capacitance of the gate oxide as well as the threshold voltage of the gate depend on the thickness of the gate oxide. Both these parameters are relevant for estimating the channel resistance of the ACCUFET.

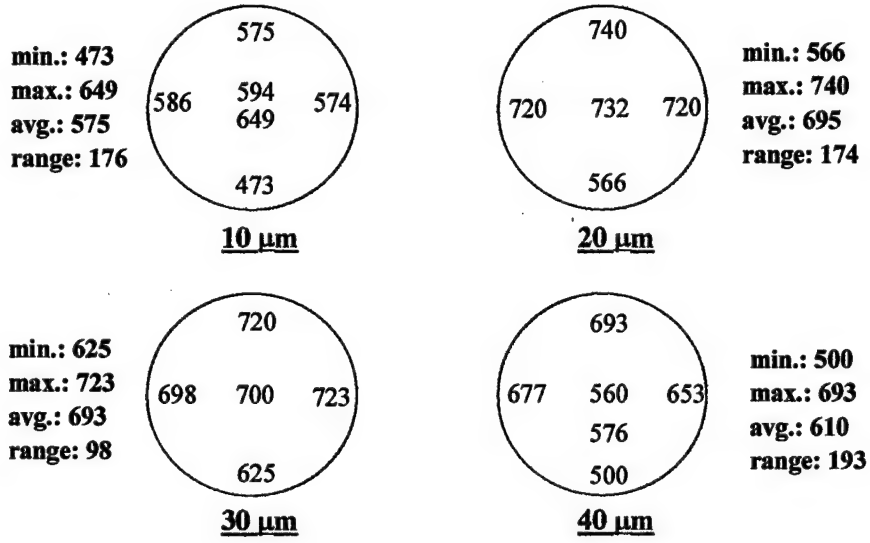


Fig. 1.5 Thickness variation of the gate oxide deposited using LPCVD. (All thickness values are in Angstroms)

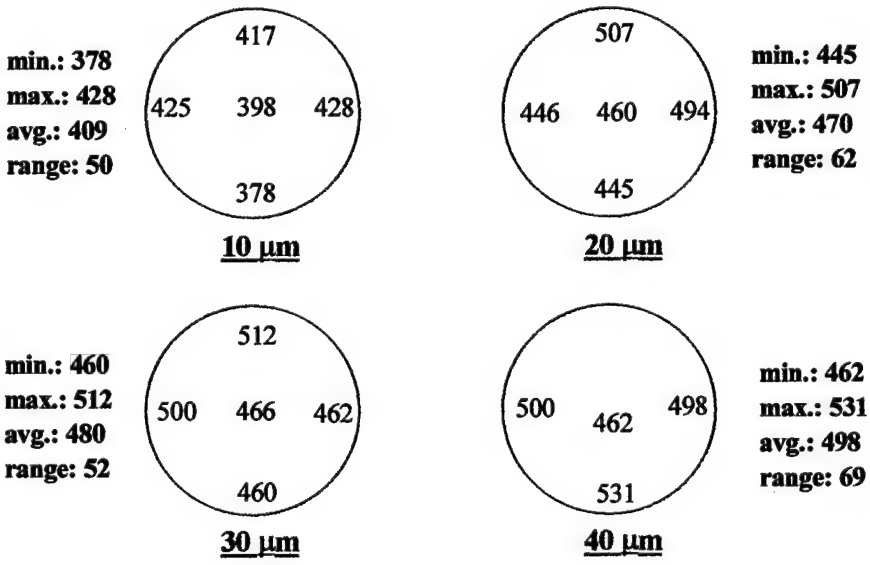


Fig. 1.6 Thickness variation of the gate oxide grown by wet oxidation. (All thickness values are in Angstroms)

On the remaining wafers, the gate oxide was grown using wet oxidation at 1100 °C followed by a re-oxidation at 950 °C to reduce density of interface states and fixed oxide charge. For this thermal oxidation, the wafers were loaded into the high temperature furnace at 800 °C on a quartz boat, and heated to 1100 °C at 5 °C/min in an oxygen ambient. The wafers were then exposed to wet nitrogen for 400 minutes, and annealed in Argon for 60 minutes at 1100 °C. Next, they were cooled to 950 °C in Argon at 3 °C/min, re-oxidized in wet nitrogen for 60 minutes, and then cooled to 800 °C at 3 °C/min in dry nitrogen. The variation of the thickness of the thermal oxide was much less than that of the LPCVD oxide, as illustrated in Fig. 1.6.

After a JT Baker clean, amorphous silicon was deposited on the wafers by LPCVD using disilane at 550 °C and 125 mTorr for 60 minutes. The deposition was done with the wafers loaded vertically on a silicon carbide boat in the center of a large quartz boat designed for holding 4" wafers. Since the silicon carbide wafers were much smaller, the flow patterns and the residence times of the reacting gas resulted in non-uniform film thicknesses with variations as high as 2000 Å across the wafer. The average about 0.35 microns. The amorphous silicon film was crystallized to polysilicon and doped in phosphorous by diffusion from phosphorous disks at 900 °C for 60 minutes in a nitrogen ambient. Next, the wafers were dipped in P-deglaze solution for 30 seconds to remove phosphosilicate glass formed on the film during the diffusion. A sheet resistance of about 80 Ω/□ was measured on the doped polysilicon films.

The polysilicon was patterned using the fifth (Poly) mask level. Polysilicon was etched by RIE for 2 minutes, using SF_6 (15 sccm) and O_2 (5 sccm) at 100 W, 60 mTorr and 15 °C. A 1 micron thick photoresist (JSR 10cp) film was used as the mask during RIE . Next, a poly-isolation oxide was grown on polysilicon using a dry/wet/dry oxidation cycle in D4 furnace in the AEMP clean room for 10/12/10 minutes at 900 °C. The wafers were loaded vertically in a quartz boat into the furnace at 750 °C in a Nitrogen (7200 sccm) ambient in 10 minutes. The temperature was ramped up to 900 °C in 30 minutes in a mixture of nitrogen (7200 sccm) and oxygen (74 sccm). The dry oxidation was done in a mixture of oxygen (1000 sccm) and hydrogen chloride (72 sccm), while the wet oxidation was done in a mixture of hydrogen (2000 sccm) and oxygen (1000 sccm). After oxidation, the wafers were cooled to 750 °C in nitrogen in 45 minutes, and the boat was removed over a period of 10 minutes.

The wafers were given a JT Baker clean, after which approximately 0.5 μm of field oxide was deposited by LPCVD using the same recipe as described previously. For the field oxide deposition, the wafers were placed horizontally and the deposition was done for 40 minutes. The contact areas were patterned using the sixth (Contact) mask level. The oxide was etched from the contact regions by RIE using a mixture of CHF_3 (25 sccm) and argon (25 sccm) at 100 W, 60 mTorr and 20 °C, for 10 minutes. Any remaining oxide was removed using BOE. The polysilicon and the oxide on the backside of the wafers were now etched off by RIE using their respective etch recipies. Then, the wafers were cleaned using JT Baker clean.

The contacts to the P+ regions were made with aluminum by a lift-off process using the seventh mask level. The photoresist solution for the lift-off process was prepared by mixing 1.5 grams of Imidazole in 50 ml of Shipley 1813 photoresist on a magnetic stirrer for 30 minutes. The solution was allowed 24 hours before use. The PR

mixture was spun on the wafers at 3500 rpm for 40 seconds. After a bake at 90 °C for 1 minute, the wafers were exposed to ultraviolet light in a Karl Suss MBJ3 aligner for 48 seconds at an intensity of 15 mW/cm^2. After exposure, the wafers were baked at 115 °C for 2 minutes, and were given a flood exposure for 2.5 minutes. The photoresist was then developed for 40 seconds. Prior to metal deposition, any remnants of the photoresist in the developed areas were removed using a lift-off descum procedure in the Asher, that used oxygen plasma at 600 mTorr and 300 W to burn off photoresist at room temperature. Aluminum was deposited on the wafers by electron beam deposition in the Edwards metal deposition system in the PSRC clean room. Approximately 3000 ❹ of aluminum was deposited, for which the electron beam was sweeped across aluminum in the crucible at an amplitude of 5 units, a frequency of 15 units, and a beam current of 60 mA for 5 minutes. The contact resistance of the aluminum contacts was improved by annealing the wafers in a forming gas ambient for 15 minutes at 700 °C.

The contacts to the N+ regions were made with a titanium/aluminum stack by a lift-off process using the eighth mask level as described in the following. Before spinning the photoresist, the wafers were degreased with acetone and methanol, rinsed with DI water, dried with nitrogen and baked for 5 minutes at 115 °C. After the photoresist was patterned for lift-off as described above, approximately 2000 ❹ of titanium was deposited using magnetron sputtering in the Edwards metal deposition system in the PSRC clean room. To obtain the required thickness, the sputtering was done at 300 W and 5 mTorr for 30 minutes. The titanium deposition was followed immediately by deposition of approximately 2000 ❹ of aluminum by electron beam evaporation in the same chamber using the above-described procedure. The contact resistance of the titanium contacts was improved by annealing the wafers in a forming gas ambient for 10 minutes at 500 °C.

The last two mask levels had been proposed and designed for improving the breakdown voltage of the devices. The focus of this thesis is primarily on the study of the forward conduction of the ACCUFETs, and hence, these two mask levels have *not* been implemented during the device fabrication. However, the details of the proposed process steps are presented here. The Schottky contacts to the N- epilayer for edge termination were proposed to be made using nickel by a lift-off process using the ninth mask level. For this purpose, approximately 500 ❹ of nickel was to be deposited using electron beam evaporation, followed by 2000 ❹ of aluminum. The tenth mask level was proposed to protect the devices with photoresist during argon ion-implantation. The argon ion implantation was to be used to form a high resistivity layer around the edges of the devices, that was expected to have improved the breakdown voltage of the devices.

1.3 Layout Design

The mask layout was designed in the 'LTL-100' layout design software with 2 μm design rules. The key technology parameters used for the design are listed in

Fig. 1.7. The layout of an ACCUFET is shown in Fig. 1.8. The edges of the device are provided with large curvatures to reduce the electric field crowding at the edge and hence, improve the blocking voltage capability. The buried P+ area in each device is laid out to result in a P+ layer from the active area of the device to its edge, with P+ fingers in the active region of the device. The gap between the P+ fingers determines the JFET width (W_{jch}) in the

Parameter	Bias, microns	Tolerance, microns
Alignment	0	+/- 2.0
Lithography (DF mask)	0.25	+/- 0.5
Lithography (LF mask)	-0.25	+/- 0.5
RIE (oxide 1 um)	0.25	+/- 0.5
RIE (poly 0.5 um)	-0.3	+/- 0.5
BOE	~ 2.tox	+/- 0.6

Fig. 1.7 Key technology parameters used during the design of device layouts.

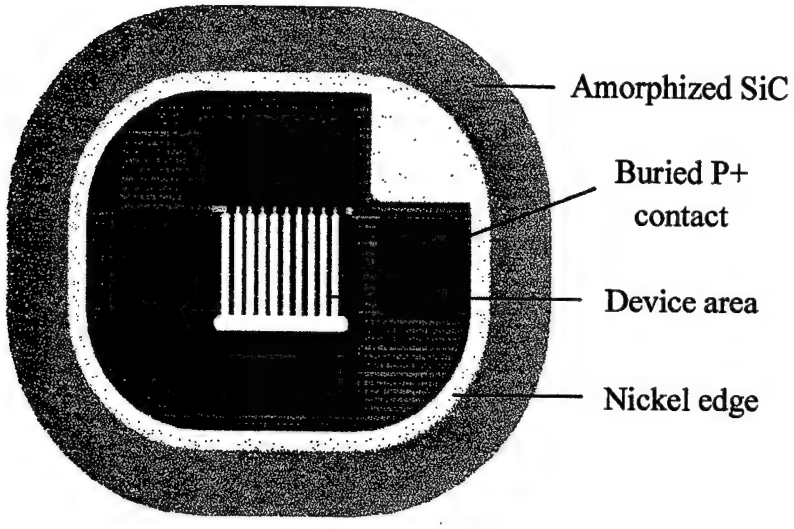
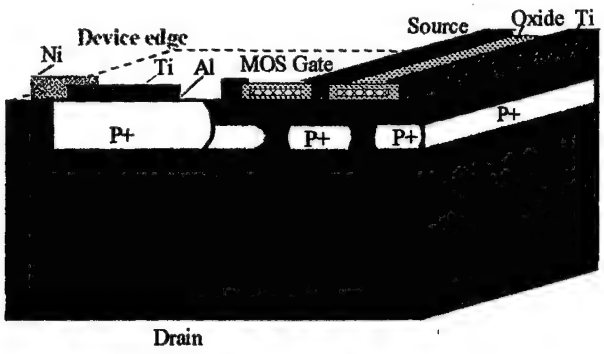


Fig. 1.8 Layout of an ACCUFET exhibiting both the device region and the edge termination.

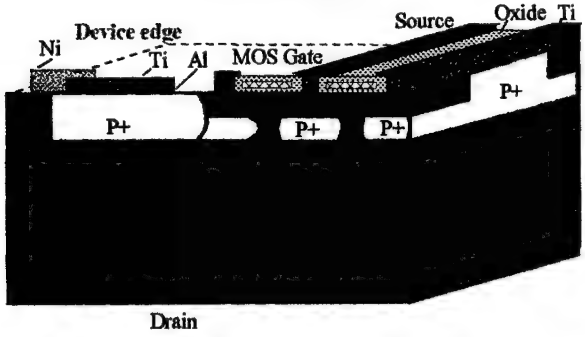
ACCUFET. This JFET width has been varied from 1.5 μm to 4.5 μm in different devices to study its impact on device behavior. The width of the P+ finger defines the MOS channel length of the device. The channel length can be calculated as half of the difference of the widths of the buried P+ finger and the N+ source finger in each cell. The channel length was varied from 1.25 μm to 4.25 μm in different devices. For these devices, the N+ source finger width was kept constant at 12 μm, and the width of the buried P+ finger was varied accordingly.

The P+ sinker area in each device was designed to extend from the edge of the buried P+ layer (which is the edge of the device) to as close to the active device area as possible. Since the activation of the implanted P+ dopants is very low in silicon carbide, such a design is expected to minimize the potential drop in the P+ region between the contact to the P+ region and the edge of the device, as well as between the contact and the buried P+ fingers in the active device area. Minimizing the potential drop between the contact and the edge is important for obtaining an effective edge termination. Similarly, minimizing the potential drop between the contact and the active device area is important

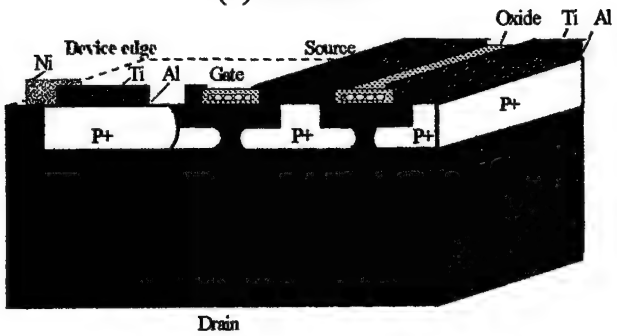
for preventing the debiasing of the parasitic JFET, which can also limit the blocking capability of the device. This design is unlike the previous design in which the P+ sinker was only along the edge of the device.



(a) Structure 1



(b) Structure 2



(c) Structure 3

Fig. 1.9 Cross-sections of the three different structures designed for fabrication of ACCUFETs.

Three different device designs were conceived for the ACCUFET (Fig. 1.9) to address the issue of the parasitic JFET regions in the device. The structure 1 is a basic design for the ACCUFET, which was also used in the previous study. In this structure, the voltage to the buried P+ fingers is applied through the contact pad to the P+ regions outside the active area of the device. In these devices, the buried P+ layer can be biased independently of the of the N+ source regions. Hence, the effect of the bias on buried P+ fingers on the device behavior could be studied using such devices. This is particularly

useful for observing the behavior of the JFET regions in the device. In these devices, however, the P+ regions and the N+ source regions need to be shorted externally during the on-state operation of the ACCUFET. In the other two device structures, the buried P+ fingers are shorted to the N+ source regions in the active device area. In structure 2, the P+ sinker implants are made to make contact with the buried P+ fingers at regular intervals along the fingers. Since the buried P+ fingers lay directly underneath the N+ source fingers, windows (5μm x 5μm) for the P+ sinker implants were incorporated within the N+ source fingers at regular intervals of 10 μm. These windows were enclosed by N+ source regions on all sides and hence, the channel density of the device did not get affected by this design. The metal contact to these P+ sinker windows was made by aluminum that was restricted in area to the P+ windows, and then, titanium was used to contact both the N+ source regions and the aluminum contacts as shown in the figure. This shorted the N+ source and the buried P+ regions orthogonally. In addition, the presence of the contacts to the buried P+ finger in the active area will be useful in suppressing any debiasing of the parasitic JFET in the device, by minimizing the potential drop across the P+ layer. Structure 3 aimed at reducing this potential drop further by incorporating P+ sinker fingers in the active area to make contact with the buried P+ fingers. The N+ source fingers lay on each side of the P+ sinker fingers. As in structure 2, aluminum was used to make contact with the P+ fingers and titanium was deposited to contact both aluminum and the N+ source fingers. However, the incorporation of the P+ fingers in the design increased the cell width and reduced the channel density of the device.

The N+ source fingers in most devices were designed to have the same width. In structures 1 and 2 only, the N+ source finger width was varied to study its effect. The minimum width required for the N+ source fingers was determined by the polysilicon-N+ source region overlap and the contact width to the N+ source regions. The gate regions in the device were defined by the polysilicon fingers. In the device structures, the metal contacting the N+ regions was intended to lie over the gate fingers and was isolated from the gate by a deposited oxide film. The deposited oxide can have pin holes which can result in gate-source shorts. Hence, a better quality polysilicon-isolation oxide was grown thermally on the polysilicon. Since the growth of the oxide consumes polysilicon, its effect was considered while determining the polysilicon finger widths and their overlap with the N+ source regions in the layout. Further, the area of the polysilicon pad into which the polysilicon fingers terminate was designed to be low, so that most of the device area could be used for P+ sinker implants as explained earlier. It was ensured that there were no P+ sinker implants under the polysilicon pad, since that could result in gate source shorts if there were any pin holes in the gate oxide. The polysilicon pad in each device was large enough to provide a good metal contact.

The contact areas were defined through the field oxide to make contact with the P+ sinker, N+ source, and polysilicon pads, as well as to open windows for the amorphization of SiC at the edge. It also opened windows in the field oxide to make contact with the N+ source fingers. The layout for aluminum contacts included large pads to make contact with the P+ sinker regions outside the active area, as well as to make contact with the P+ sinker regions inside the active area in structures of types 2 and 3.

Device ID	Lch (μm)	Wjch (μm)	Wn+ (μm)	Wp (μm)	Wcell (μm)
rmos211	2.25	4.5	12.0	16.5	21.0
rmos201	2.25	3.5	12.0	16.5	20.0
rmos191	2.25	2.5	12.0	16.5	19.0
rmos181	2.25	1.5	12.0	16.5	18.0
rmos182	1.25	3.5	12.0	14.5	18.0
rmos221	3.25	3.5	12.0	18.5	22.0
rmos241	4.25	3.5	12.0	20.5	24.0
rmos101	2.0	2.0	4.0	8.0	10.0
rmos242	3.25	3.5	14.0	20.5	24.0
rmos262	3.25	3.5	16.0	22.5	26.0

(a) Design matrix for structure 1.

Device ID	Lch (μm)	Wjch (μm)	Wn+ (μm)	Wp (μm)	Wcell (μm)
rmos211s2	2.25	4.5	12.0	16.5	21.0
rmos201s2	2.25	3.5	12.0	16.5	20.0
rmos191s2	2.25	2.5	12.0	16.5	19.0
rmos181s2	2.25	1.5	12.0	16.5	18.0
rmos182s2	1.25	3.5	12.0	14.5	18.0
rmos221s2	3.25	3.5	12.0	18.5	22.0
rmos241s2	4.25	3.5	12.0	20.5	24.0
rmos101s2	2.0	2.0	4.0	8.0	10.0
rmos242s2	3.25	3.5	14.0	20.5	24.0
rmos262s2	3.25	3.5	16.0	22.5	26.0

(b) Design matrix for structure 2.

Device ID	Lch (μm)	Wjch (μm)	Wn+ (μm)	Wp (μm)	Wcell (μm)
rmos211s3	2.25	4.5	12.0	19.5	24.0
rmos201s3	2.25	3.5	12.0	19.5	23.0
rmos191s3	2.25	2.5	12.0	19.5	22.0
rmos181s3	2.25	1.5	12.0	19.5	21.0
rmos182s3	1.25	3.5	12.0	17.5	21.0
rmos221s3	3.25	3.5	12.0	21.5	25.0
rmos241s3	4.25	3.5	12.0	23.5	27.0

(c) Design matrix for structure 3.

Fig. 1.10 Design matrices for the three different structures designed for fabrication of ACCUFETs.

The titanium pads were used to make contact with the N+ source regions and the polysilicon pad. The pad that made contact with the N+ regions was designed to be large in area. The use of contact fingers in the oxide to the N+ fingers and a large titanium pad that spread over the gate fingers while making contact with the N+ fingers, eliminated the need for creating thin metal finger contacts to the source fingers by a lift-off process, whose success has been found to be unpredictable in the past. Further, the large pad allows the use of multiple probes for contact during measurements such as the Kelvin measurements. The aluminum pads for contact to the P+ regions are expected to lose shape after a high temperature post-metallization anneal that is used for improving the contact resistance. Hence, the titanium pads are also designed to cover over the aluminum

pads. The mask for nickel was designed such that nickel Schottky contact would extend up to 20 μm beyond the device edge. A contact pad was also provided with the nickel edge to allow biasing of this Schottky contact. The layout of the final mask was designed to protect the devices from the low energy argon implants used for amorphization of silicon carbide by using photoresist as the mask. These implants are intended to amorphize the region between the Schottky contact at the device edge and the field oxide which will lie at a distance of 100 μm from the edge of the Schottky metal.

As mentioned earlier, the individual device designs were appropriately chosen to study the effect of variation of width of JFET region (W_{jch}), channel length (L_{ch}) and N+ source width (W_{N+}) on device performance. The design matrix for the devices of each type of structure is shown in Fig. 1.10. W_{jch} was varied between 1.5 and 4.5 μm and L_{ch} was varied between 1.25 and 4.25 μm that resulted in a corresponding change in the width of the buried P+ finger (W_p). W_{n+} was varied between 12 and 16 μm. The cell widths (W_{cell}) varied from 18 to 26 μm. In Fig. 1.11, the complete layout of the die is shown. Apart from the various designs for the ACCUFETs and the test element groups, several designs for Junction Field Effect Transistors (JFET) and Junction Barrier Schottky (JBS) diodes whose fabrication compatible with the ACCUFET process flow, are shown.

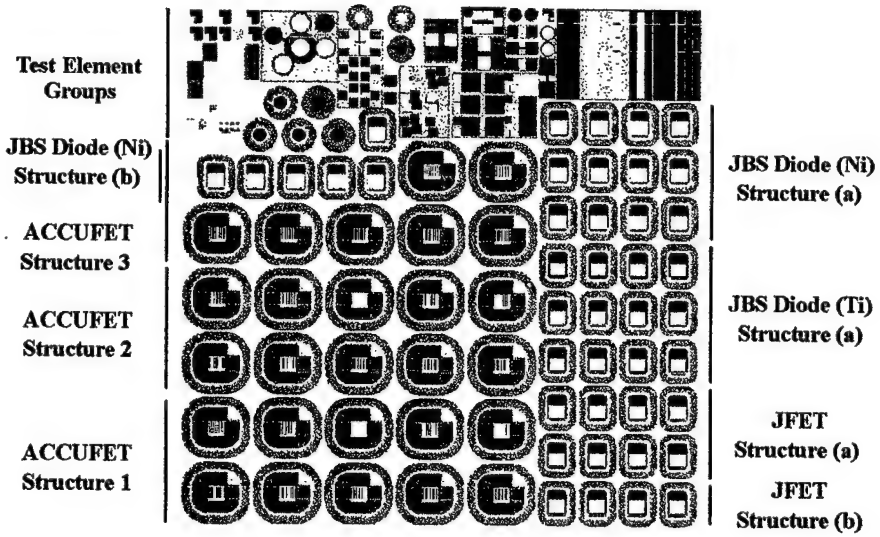


Fig. 1.11 Complete layout of all the devices.

1.4 Process-induced variations in device dimensions

The dimensions of the fabricated devices are never the same as those on the mask. This is due to the bias and tolerance values expected for features after different process steps involved in the fabrication of these devices. This can influence the performance of the resultant devices, and hence it is important to understand the process-induced variations in the size of the critical device design parameters. During the mask design, the bias and tolerance values (Fig. 1.7) were used to determine the limits on various feature sizes that are required to make working devices. Two design parameters, that are

particularly of interest in determining the forward conduction characteristics of the ACCUFETs, are the width of the buried JFET region (W_{jch}) and the channel length (L_{ch}).

The width of the buried JFET region (W_{jch}) in the ACCUFET is the gap between two buried P+ fingers. As described in the process sequence, the buried P+ fingers were formed by boron implants into SiC through windows created in a thick deposited oxide that masked the implants in the rest of the wafer. These windows were created by photolithography, followed by RIE and BOE of the oxide. Hence, if x (μm) is the width of the buried P+ finger on the mask, then the buried P+ finger width (W_p) on the wafer is given by

$$Wp = x + \sum bias \pm \sqrt{\sum (tolerance)^2} \tag{1.1}$$

where,

$$\sum bias = litho\_bias + RIE\_bias + BOE\_bias \tag{1.2}$$

$$\sum (tolerance)^2 = (litho\_tol.)^2 + (RIE\_tol.)^2 + (BOE\_tol.)^2 \tag{1.3}$$

From the process sequence and the key technology parameters, the bias values for lithography, RIE and BOE can be determined to be 0.25 μm, 0.325 μm and 0.6 μm, respectively. Thus, from Eq. (1.1), W_p can range between (x + 2.1) and (x + 0.25) μm. Hence, if W_{jch} is the width of the buried JFET region on the mask, then on the wafer, this width can vary between (W_{jch} - 2.1) μm and (W_{jch} - 0.25) μm.

The channel in the ACCUFET is formed between the edges of the buried P+ layer and the N+ source layer. Hence, the channel length is affected by the bias and the tolerance values for the two layers as well as the alignment tolerance between the layers. The lithography biases from the two layers act in the same direction, and their effects cancel out. Hence, if L_{ch} is the channel length on the mask, then, the actual channel length on the wafer ($L_{ch,act}$) is given by

$$L_{ch,act} = L_{ch} + \sum bias \pm \sqrt{\sum (tolerance)^2} \tag{1.4}$$

where,

$$\sum bias = \frac{RIE\_bias}{2} + \frac{BOE\_bias}{2} \tag{1.5}$$

$$\sum (tolerance)^2 = \left(\frac{litho\_tol.}{2}\right)^2_{P+} + \left(\frac{litho\_tol.}{2}\right)^2_{N+} + \left(\frac{RIE\_tol.}{2}\right)^2 + \left(\frac{BOE\_tol.}{2}\right)^2 + (Align\_tol.)^2 \tag{1.6}$$

From these calculations, it can be shown that the actual channel length on the wafer can vary between (Lch - 1.14) μm and (Lch + 3) μm.

1.5 Test element groups

The test element groups (TEG) are used to characterize the process and gain insights about the device behavior. The number of test element groups that were used to understand the behavior of the fabricated ACCUFETs are described here.

The *lateral MOSFET* is used to determine the effective accumulation channel mobility and the gate threshold voltage. This device is comprised of N+ source and drain regions, a polysilicon gate and a buried P+ layer. Just as in an ACCUFET, during device operation, the buried P+ layer and the N+ source in the lateral MOSFET are connected to

ground, and a positive bias is applied to the drain. At zero gate bias, the n-type region between the gate and the buried P+ layer is fully depleted, making the MOSFET normally-off. When a positive gate bias greater than the threshold voltage is applied to the gate, the electrons flow from the source to the drain through an accumulation channel created at the gate. The width and length of the gate of this lateral MOSFET are 170 μm and 80 μm, respectively.

The *lateral resistors* are used to measure the sheet resistance of the buried P+ layer, the P+ sinker layer, the N+ source layer and the polysilicon film. They are two terminal lateral devices shaped like dumbbells. The sheet resistance can be obtained by measuring the resistance of the thin current-carrying portion between the contact pads and dividing it by the number of squares (length to width ratio) in that portion. The resistors are designed to have a length to width ratio of 10 in the thin current carrying region.

Vertical p-n junction diodes are included to estimate the forward conduction and the reverse blocking characteristics of the buried p-n junction in the ACCUFET. These diodes are 150 μm in diameter. *Schottky diodes* made from titanium (150 μm diameter) on N- epilayer were used to extract the resistance of the drift region. The contact resistance to the N+ source region, which contributes to the specific on-resistance of the device, can be measured using a Kelvin structure [3] with a contact area of 3 μm x 3 μm.

1.6 References

1. P. M. Shenoy, *High Voltage Buried Junction Vertical Silicon Carbide Field Effect Transistors*, Ph.D. Thesis, 1997.
2. S. Sridevan, *Characterization of Inversion Layers on SiC*, Ph.D. Dissertation, 1998.
3. D. K. Schroder, *Semiconductor Material and Device Characterization*, John Wiley & Sons, 2nd edition, 1998.

High Voltage 4H-SiC ACCUFET Experimental Results

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Abstract

The forward conduction characteristics of 4H-SiC ACCUFETs, fabricated on starting material with different epilayer doping and thickness values, are presented. The effect of the key design parameters, such as the channel length, the buried JFET region width, and the gate oxide thickness, and the effect of their process-induced variations on the performance of these devices are discussed. Further, an analytical model developed previously for the on-resistance of the devices has been verified with the aid of the experimental results.

1.1 Introduction

In the previous reports [1], a new fabrication run for fabricating ACCUFETs on starting material of varying epilayer thickness and doping values, corresponding to a range of breakdown voltages, was discussed. The properties of the starting material for the high voltage devices are important for determining the device performance and for optimizing the device designs. In order to develop good device designs, it was essential to understand the device physics for predicting the implications of the process and device design parameters on the device performance. Hence, the device physics and the operation of the planar ACCUFET were discussed in detail, and the effects of key device design parameters on device characteristics were described with the aid of two-dimensional simulations [2]. In addition, an analytical model for evaluating the different components of the on-resistance of the planar ACCUFET was presented.

Here, the forward conduction characteristics of the fabricated 4H-SiC ACCUFETs are presented. The effect of the key design parameters and of their process-induced variations on the performance of these devices are discussed. Further, the analytical model developed for the on-resistance of the devices has been verified with the aid of the experimental results.

1.2 Forward conduction

The current-voltage (I-V) characteristics of the ACCUFETs were measured using Keithley source measure units. These forward conduction characteristics were obtained by connecting the N+ source and the buried P+ contact pads to ground, applying a positive bias to the drain (wafer bottom) and the gate. To obtain a family of curves, the drain bias was typically increased from zero to 100 V, while the gate bias was typically stepped from 0 V to 32 V.

As discussed in the process sequence [1], the devices were fabricated using an LPCVD oxide (LTO) as well as a thermal oxide for the gate. With each type of gate oxide, the devices were fabricated on 4 wafers of varying epilayer thickness and doping values. The I-V characteristics of the ACCUFETs on all the eight wafers were measured. There were 27 unique designs of the ACCUFETs on each die. Because of the small size (1.375 inch diameter) and the large cost of the silicon carbide wafers, approximately only nine measurable devices of each design could be fabricated. Moreover, the process technology for the fabrication of devices on silicon carbide is still not mature, and the quality of the starting material is not uniform. This has resulted in poor to moderate yields on the devices, and some process-induced variations, as discussed later. Hence, only the best measured characteristics were chosen for the device analysis, and no statistical analysis could be performed.

The I-V measurements were done both at room temperature and at 200 °C. The high temperature measurements on silicon carbide devices are of interest because one of the reasons for switching from silicon to silicon carbide technology is the applicability of silicon carbide devices to high temperature environments. Further, the device characteristics of silicon carbide MOSFETs have been found to alter significantly at high temperatures, as discussed later.

Two important device design parameters for an ACCUFET are the channel length and the width of the buried JFET region. The I-V characteristics of the ACCUFETs were grouped and studied by the channel lengths and the JFET widths in each device type on each wafer. It was observed that the ACCUFETs with a *thermal* gate oxide exhibited poor performance and large gate leakage currents. This is illustrated in Fig. 1.1 through Fig. 1.6, which show the device characteristics of ACCUFETs on the 40 μm epilayer. The characteristics of the thermal gate oxide ACCUFETs on the other wafers were similar. In contrast, the *deposited* gate oxide resulted in good working devices with negligible gate leakage, as illustrated from Fig. 1.7 through Fig. 1.54 (Fig. 1.1 through Fig. 1.54 are compiled in the *Appendix*). Hence, a detailed analysis of the device performance was done only on the ACCUFETs with a deposited gate oxide.

1.3 Materials considerations

1.3.1 Effective channel mobility

The effective channel mobility at SiO_2/SiC interfaces are much less than half the bulk mobility which is typically achieved on silicon [3]. The effective channel mobility is reported to be small at room temperature and to increase with temperature with an activation energy of 0.3 eV [4]. This is attributed to a high density of interface traps (D_{it}) near the conduction band edge. The effective channel mobility is not a true mobility because a fraction of the charge produced by the gate voltage is trapped. The effective channel mobility increases rapidly with temperature because the number of electrons in the trap states decreases and the concentration of free electrons in the surface inversion/accumulation layer in the conduction band increases with temperature according to Fermi-Dirac Statistics. The activation energy exhibited by the mobility corresponds to the location of the high density of interface states from the conduction band in the band diagram. Recent studies have shown that the Hall mobilities of inversion layers are much larger than the apparent drift mobilities, because of anomalously low free carrier concentrations due to high D_{it} near the conduction band edge [5].

1.3.2 Threshold voltage

The threshold voltage is an important parameter for estimating the channel resistance. The threshold voltage in the ACCUFET is given by [6]

$$V_{th} = \phi_{ms} + \left(\frac{\varepsilon_s V_{bi}}{\varepsilon_{ox} W_{db}} + \frac{q N_D W_{db}}{2 \varepsilon_0 \varepsilon_{ox}} \right) t_{ox} - \frac{Q_{eff} . t_{ox}}{\varepsilon_0 \varepsilon_{ox}} \qquad (1.1)$$

where, ϕ_{ms} is the work function difference between the gate material and the lightly doped N- region under the gate. The second term represents the effect of the built-in potential of the buried P+/N junction on the threshold voltage. Here, V_{bi} is the built-in potential of the P+/N junction, N_D is the doping of the N- base region, t_{ox} is the thickness of the gate oxide, and W_{db} is the width of the N- region between the MOS gate and the buried P+ layer. The third term represents the effect of the effective density of the sheet oxide charge, Q_{eff} C/cm^2, located at the oxide-semiconductor interface. Q_{eff} is assumed to be positive in Eq. (1.1).

The calculation of the individual terms in the above equation illustrate the contribution of these individual components to the measured threshold voltage in the fabricated ACCUFETs. The 4H-SiC ACCUFETs use highly doped n-type polysilicon for the gate. The doping of the lightly doped n-type 4H-SiC under the gate can be assumed to be $1x10^{16}$ cm^{-3}, which is the doping of the 10 μm epilayer used for device fabrication. Hence, at room temperature, ϕ_{ms} for this MOS system can be calculated to be 0.265 V. This value is negligible compared to the typical measured threshold voltage of 13.5 V as shown in section 1.4. Thus, the threshold voltage of these ACCUFETs can be assumed to increase linearly with the thickness of the gate oxide. Further, using a gate oxide thickness of 575 Å, the built-in potential of 2.96 V, and W_{db} value of 0.2 μm, the second term in Eq. (1.1) can be calculated to be 1.85 V. If the contribution from the gate oxide charge is ignored, then the threshold voltage is calculated to be 2.11 V, which is consistent with that obtained from the simulations [2]. However, the measured threshold voltage is much larger than this value, and this can be attributed to a large negative effective oxide charge. For an n-type MOS capacitor, the Fermi level is near the conduction band at flat band at most of the interface states and border traps are occupied by electrons. This negative charge subtracts from the *true* positive fixed oxide charge, yielding an effective negative charge.

1.3.3 Material properties

For device analysis, it is essential to evaluate the properties of the working material. In this section, important material properties used in the analytical model for the on-resistance are discussed. These material properties are evaluated at room temperature as well as at 200 °C.

The intrinsic carrier concentration, n_i, is given by

$$n_i = \sqrt{N_C N_V}\, exp\left(-\frac{E_g}{2kT}\right) \tag{1.2}$$

where, E_g is the band gap, and N_C and N_V are the effective density of states in the conduction band and the valence band, respectively. For 4H-SiC at 300 K, N_C, N_V and E_g are $1.23x10^{19}$ cm^{-3}, $4.58x10^{18}$ cm^{-3}, and 3.26 eV, respectively. Both N_C and N_V increase with temperature and are proportional to $T^{1.5}$. The intrinsic carrier concentration is used to evaluate the built-in potential V_{bi} of a p-n junction, which in turn can be used to evaluate the depletion at the junction [2].

The conductivity of a semiconductor is expressed at $q\mu_n n_D$, where μ_n is the bulk mobility of the semiconductor and n_D is the carrier concentration. For 4H-SiC, the bulk mobility of electrons in an n-type 4H-SiC in the c-axis is given by [7]

$$\mu_n = \frac{947}{1+\left(\frac{N_D}{1.94\times10^{17}}\right)^{0.61}} \tag{1.3}$$

In the temperature range of our interest, the mobility reduces with temperature as $T^{-2.4}$. The carrier concentration can be calculated, for nitrogen doped n-type silicon carbide, using an ionization energy of 0.1 eV.

Apart from these material properties, it is essential to know the process dependent electrical properties such as the effective channel mobility, the threshold voltage, the N+ source sheet resistance, and the source contact resistance, which can be measured using the test element groups.

1.4 Test element groups

The effective accumulation channel mobility and the threshold voltage were extracted from the output characteristics of the lateral MOSFETs. As illustrated in Fig. 1.1 and Fig. 1.2, the I-V curves were obtained for lateral MOSFETs on each epilayer at both room temperature as well as at 200 °C. The gate voltage was varied from 0 V, in steps of 4 V, to 32 V. The transfer characteristics for each case were obtained by plotting the square root of the drain current at a drain bias of 20 V, against the gate voltage. The transfer characteristics plotted at two different temperatures are shown in Fig. 1.57 and Fig. 1.58. The effective channel mobility was calculated using the slope of the I_D-V_G curve at large gate biases as the following

$$\mu_{na} = \frac{2L_{ch}}{C_{ox}W_{ch}}\left(\frac{\Delta\sqrt{I_D}}{\Delta V_G}\right)^2 \qquad (1.4)$$

where, L_{ch} is the channel length, W_{ch} is the channel width, and C_{ox} is the oxide capacitance. For the lateral MOSFET, L_{ch} and W_{ch} were 80 μm and 170 μm, respectively. The threshold voltage is obtained from the intercept of the tangential line to the I-V curve used for calculating the mobility, with the V_G axis.

Both the effective channel mobility and the threshold voltage were obtained for each wafer at each temperature. Due to the non-uniformity in the material quality, the measurements were done on a MOSFET near the area on the device wafer where most good working devices were located. At room temperature, the effective channel mobilities on the 10 μm, 20 μm, 30 μm and 40 μm epilayers were 0.27 cm^2/Vs, 0.03 cm^2/Vs, 0.05 cm^2/Vs and 0.07 cm^2/Vs, respectively. At 200 °C, these values increased to 1.57 cm^2/Vs, 0.39 cm^2/Vs, 0.53 cm^2/Vs and 0.70 cm^2/Vs, respectively. Similarly, the threshold voltages on the 10 μm, 20 μm, 30 μm and 40 μm epilayers were 13.5 V, 19.0 V, 17.0 V and 17.0 V, respectively. At 200 °C, these values reduced to 7.5 V, 17.5 V, 10.5 V and 14.0 V, respectively.

The sheet resistance of the N+ source region was obtained by measuring the resistance across the N+ resistor. At room temperature, the sheet resistance values of the N+ source regions on the 10 μm, 20 μm, 30 μm and 40 μm epilayers were 3898 Ω/□, 7000 Ω/□, 7143 Ω/□, and 9000 Ω/□, respectively. At 200 °C, these values reduced to 893 Ω/□, 4167 Ω/□, 3571 Ω/□, and 4167 Ω/□, respectively. The reduction in the resistance of the N+ source regions is attributed to higher carrier concentration due to increased ionization at the higher temperature. The contact resistance of the titanium contacts to the N+ source regions was evaluated by a Kelvin measurement on the contact resistance test structure. The contact resistance on all wafers was found to be about 1 $m\Omega cm^2$ at room temperature and about 0.6 $m\Omega cm^2$ at 200 °C.

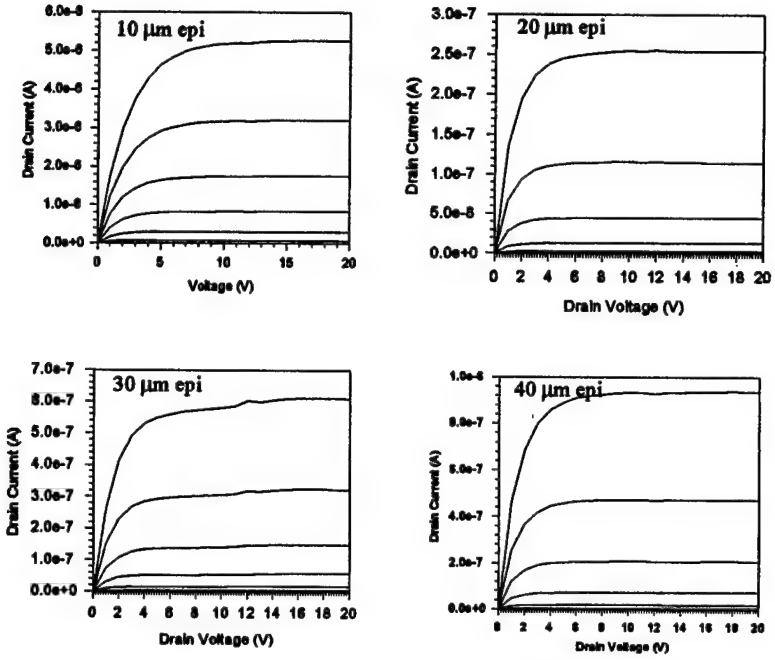

Fig. 1.1 Output characteristics of lateral MOSFETs on different epilayers at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V).

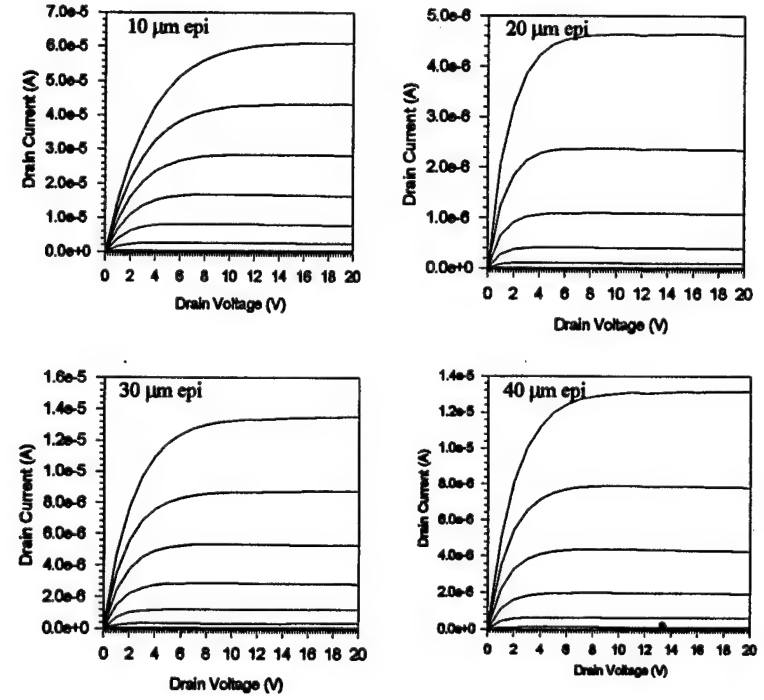

Fig. 1.2 Output characteristics of lateral MOSFETs on different epilayers at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V).

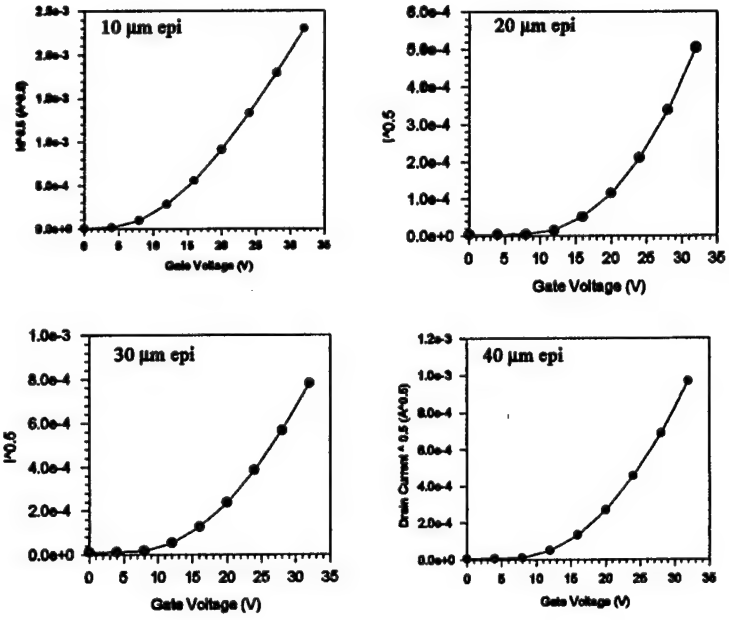

Fig. 1.3 Transfer characteristics of lateral MOSFETs on different epilayers at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V).

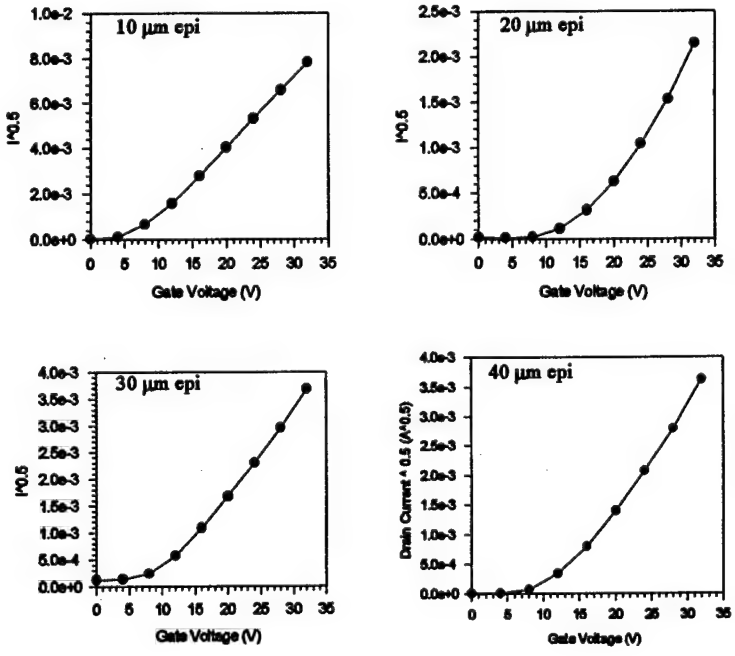

Fig. 1.4 Transfer characteristics of lateral MOSFETs on different epilayers at a temperature of 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V).

1.5 Device Analysis

1.5.1 Output characteristics

The output characteristics of the ACCUFETs were measured on all the wafers with *deposited* gate oxide at room temperature as well as at 200 °C. The effect of the width of the JFET region, the channel length, the device structure type, the temperature and the epilayer doping and thickness, on the output characteristics were documented and are presented in Fig. 1.7 through Fig. 1.54. The following observations can be made from these I-V characteristics :

1. Almost all ACCUFETs exhibit enhancement-mode MOSFET-like characteristics with a large positive threshold voltage and a relatively flat saturation region.
2. The drain currents at 200 °C are about an order of magnitude higher than those at room temperature (for example, compare Fig. 1.31 with Fig. 1.37).
3. The threshold voltage reduces with temperature (for example, compare Fig. 1.31 with Fig. 1.37).
4. The ACCUFETs with a buried JFET width of less than 3.5 μm exhibit an offset drain voltage until which the drain current is zero (for example, see Fig. 1.19,W_{jch}=2.5 μm). For drain voltages larger than this offset voltage, the drain current increases exponentially and then, exhibits MOSFET-like characteristics with linear and saturation regions. The offset voltages are greater than 100 V in some ACCUFETs with a JFET width of 1.5 μm (for example, see Fig. 1.19,W_{jch}=1.5 μm). Smaller offset voltages are observed at larger JFET widths when the doping of the epilayer is low (for example, compare Fig. 1.19,W_{jch}=2.5 μm and W_{jch}=3.5 μm). The offset voltage is zero for ACCUFETs on all wafers when the JFET width is 4.5 μm. For the 10 μm epilayer, which has the highest doping among the starting materials, the offset voltage is nearly zero at all JFET widths except the smallest width of 1.5 μm (for example, see Fig. 1.7). As explained previously, the offset voltage is caused by the pinching-off of the JFET regions by spreading of depletion from the buried P+ layer, resulting in a triodelike behavior of the devices. Hence, this behavior is very apparent at small JFET widths and low epilayer doping values. The offset voltages correlate with the JFET width in most devices (for example, see Fig. 1.31 through Fig. 1.33), and any deviations from the expected offset voltage values could be attributed to the process-induced variations of the JFET width.
5. The drain currents increase when the channel length is reduced (for example, see Fig. 1.22 through Fig. 1.24). The ACCUFETs with a channel length of 1.25 μm exhibit much larger saturation currents than the those with longer channels and exhibit a strong dependence on drain bias due to channel length modulation (for example, see Fig. 1.10, L_{ch}=1.25 μm). The channel length modulation can be observed to be negligible in the long channel ACCUFETs (for example, see Fig. 1.10, L_{ch}=4.25 μm).
6. Some of the ACCUFETs on the 10 μm epilayer, which has the highest doping, exhibit significant drain current even at zero gate bias (see Fig. 1.7, W_{jch}=2.5 μm). This current is attributed to leakage through a parasitic surface JFET. For the ACCUFET to be normally-off, this parasitic surface JFET needs to be completely pinched off by the built-in potential of the P+/N junction and the MOS gate. However, this JFET may not be completely pinched-off when the N- doping is high, resulting in significant

drain currents even when the gate bias is zero. This effect is further discussed in section 1.6.

1.5.2 Specific on-resistance

The analytical model for determining the specific on-resistance of an ACCUFET has been discussed in detail in [2]. Here, this model is applied to estimate the contributions of the individual on-resistance components to the measured device on-resistance. The material and device parameters required for making these estimates are gathered either from the test element groups or from literature, as explained earlier. Only the ACCUFETs which exhibited a zero offset voltage were considered for this analysis, because the on-resistance can be defined only for such devices. Based on this consideration, the ACCUFETs with a JFET width of 4.5 μm were selected from all the wafers. In addition, from the 10 μm thick and the 40 μm thick epilayers, devices with a JFET width of 3.5 μm could also be selected. This allowed the study of the effect of the channel length variation on the on-resistance of the ACCUFETs on these two wafers.

Before estimating the on-resistance components, it was recognized that the process-induced variations in the channel length, the JFET width and the gate oxide thickness could result in significant deviations of the measured ACCUFET on-resistance values from those expected. The process-induced variations in the channel length and the JFET width were estimated as discussed in [1]. The variations in the gate oxide thickness (t_{ox}) effect the channel resistance. The threshold voltage (V_T) increases linearly with increase in t_{ox}, while the gate oxide capacitance (C_{ox}) decreases linearly with t_{ox}. Since the channel resistance is inversely proportional to (V_G-V_T) and C_{ox}, it increases with t_{ox}. In order to estimate a range for the expected values of the measured on-resistance based on these considerations, three combinations of the channel length (L_{ch}), the JFET width (W_{jch}), and the gate oxide thickness (t_{ox}) were chosen for each of the selected devices from each wafer, as follows :

1. $L_{ch,mask}$, $W_{jch,mask}$ and $t_{ox,average}$: to estimate the on-resistance if the expected device design is obtained from the fabrication.
2. $L_{ch,min}$, $W_{jch,max}$ and $t_{ox,min}$: to estimate the minimum on-resistance.
3. $L_{ch,max}$, $W_{jch,min}$ and $t_{ox,max}$: to estimate the maximum on-resistance.

The individual specific resistance components were evaluated based on our model for these three cases for all the selected devices at both room temperature as well as at 200 °C, as detailed in Fig. 1.59 through Fig. 1.62. The substrate resistance, not shown in these tables, was calculated to be only 0.045 $m\Omega.cm^2$ based on the substrate resistivity (ρ_{sub}) value of 0.015 Ω.cm, thickness of 300 μm and current spreading factor (n_{cs}) of 10 obtained from simulations.

Note that the channel resistance in all the devices is dominant and is at least one order of magnitude larger than the remaining resistance components. The large channel resistance component is due to a small effective channel mobility and large threshold voltage. At higher temperature, the channel resistance drops considerably due to an increase in the effective channel mobility and a reduction in the threshold voltage, resulting in much lower device on-resistance. It is interesting to note that the channel mobilities on the 10 μm epilayer are higher than those on the thicker epilayers. The epitaxy of the

At room temperature

Device	Lch (um)	Wjch (um)	tox (A)	Rcs	Rn+	Rchannel	Rjfet	Rdrift	Ron,estimated	Ron,measured
#5	1.25	3.50	575.00	6.00	8.42	783.39	0.97	2.10	801.33	133.40
	0.11	3.25	473.00	6.00	8.42	50.21	1.08	2.21	68.37	
	4.25	1.40	649.00	6.00	8.42	3317.91	8.44	4.36	3345.59	
#2	2.25	3.50	575.00	6.67	9.36	1566.78	1.08	2.34	1586.67	2055.08
	1.11	3.25	473.00	6.67	9.36	562.96	1.20	2.45	583.09	
	5.25	1.40	649.00	6.67	9.36	4554.00	9.38	4.84	4584.70	
#6	3.25	3.50	575.00	7.33	10.29	2489.45	1.19	2.57	2511.28	179.46
	2.11	3.25	473.00	7.33	10.29	1177.14	1.33	2.70	1199.24	
	6.25	1.40	649.00	7.33	10.29	5963.57	10.32	5.33	5997.29	
#7	4.25	3.50	575.00	8.00	11.23	3551.38	1.29	2.80	3575.15	2014.33
	3.11	3.25	473.00	8.00	11.23	1892.76	1.45	2.95	1916.83	
	7.25	1.40	649.00	8.00	11.23	7546.63	11.26	5.81	7583.37	
#15	1.25	3.50	575.00	6.00	8.42	783.39	0.97	2.10	801.33	267.90
	0.11	3.25	473.00	6.00	8.42	50.21	1.08	2.21	68.37	
	4.25	1.40	649.00	6.00	8.42	3317.91	8.44	4.36	3345.59	
#12	2.25	3.50	575.00	6.67	9.36	1566.78	1.08	2.34	1586.67	1778.20
	1.11	3.25	473.00	6.67	9.36	562.96	1.20	2.45	583.09	
	5.25	1.40	649.00	6.67	9.36	4554.00	9.38	4.84	4584.70	
#16	3.25	3.50	575.00	7.33	10.29	2489.45	1.19	2.57	2511.28	1026.76
	2.11	3.25	473.00	7.33	10.29	1177.14	1.33	2.70	1199.24	
	6.25	1.40	649.00	7.33	10.29	5963.57	10.32	5.33	5997.29	
#17	4.25	3.50	575.00	8.00	11.23	3551.38	1.29	2.80	3575.15	7732.76
	3.11	3.25	473.00	8.00	11.23	1892.76	1.45	2.95	1916.83	
	7.25	1.40	649.00	8.00	11.23	7546.63	11.26	5.81	7583.37	
#25	1.25	3.50	575.00	7.00	9.82	913.96	1.13	2.45	934.82	640.42
	0.11	3.25	473.00	7.00	9.82	58.58	1.27	2.58	79.69	
	4.25	1.40	649.00	7.00	9.82	3870.90	9.85	5.09	3903.11	
#22	2.25	3.50	575.00	7.67	10.76	1801.80	1.24	2.69	1824.60	1592.82
	1.11	3.25	473.00	7.67	10.76	647.40	1.39	2.82	670.49	
	5.25	1.40	649.00	7.67	10.76	5237.10	10.79	5.57	5272.33	
#26	3.25	3.50	575.00	8.33	11.69	2828.92	1.35	2.92	2853.66	869.83
	2.11	3.25	473.00	8.33	11.69	1337.66	1.51	3.07	1362.71	
	6.25	1.40	649.00	8.33	11.69	6776.78	11.73	6.06	6815.04	
#27	4.25	3.50	575.00	9.00	12.63	3995.30	1.46	3.15	4021.99	2165.13
	3.11	3.25	473.00	9.00	12.63	2129.35	1.63	3.31	2156.37	
	7.25	1.40	649.00	9.00	12.63	8489.96	12.67	6.54	8531.24	
#1	2.25	4.50	575.00	7.00	9.82	1645.12	0.80	2.08	1665.27	1792.86
	1.11	4.25	473.00	7.00	9.82	591.11	0.86	2.16	611.40	
	5.25	2.40	649.00	7.00	9.82	4781.70	2.11	3.17	4804.25	
#11	2.25	4.50	575.00	7.00	9.82	1645.12	0.80	2.08	1665.27	1453.07
	1.11	4.25	473.00	7.00	9.82	591.11	0.86	2.16	611.40	
	5.25	2.40	649.00	7.00	9.82	4781.70	2.11	3.17	4804.25	
#21	2.25	4.50	575.00	8.00	11.23	1880.14	0.91	2.37	1903.10	1799.12
	1.11	4.25	473.00	8.00	11.23	675.55	0.98	2.46	698.67	
	5.25	2.40	649.00	8.00	11.23	5464.80	2.41	3.62	5490.51	

At 200 °C

Device	Lch (um)	Wjch (um)	tox (A)	Rcs	Rn+	Rchannel	Rjfet	Rdrift	Ron,estimated	Ron,measured
#5	1.25	3.50	575.00	3.60	1.93	101.73	2.67	5.92	115.90	32.22
	0.11	3.25	473.00	3.60	1.93	6.98	2.98	6.22	21.76	
	4.25	1.40	649.00	3.60	1.93	406.41	20.58	11.94	444.49	
#2	2.25	3.50	575.00	4.00	2.14	203.46	2.97	6.58	219.20	400.79
	1.11	3.25	473.00	4.00	2.14	78.32	3.31	6.91	94.72	
	5.25	1.40	649.00	4.00	2.14	557.81	22.86	13.26	600.13	
#6	3.25	3.50	575.00	4.40	2.36	323.28	3.26	7.24	340.58	70.24
	2.11	3.25	473.00	4.40	2.36	163.76	3.64	7.60	181.80	
	6.25	1.40	649.00	4.40	2.36	730.47	25.15	14.59	777.01	
#7	4.25	3.50	575.00	4.80	2.57	461.18	3.56	7.89	480.05	222.75
	3.11	3.25	473.00	4.80	2.57	263.31	3.97	8.29	282.99	
	7.25	1.40	649.00	4.80	2.57	924.38	27.43	15.92	975.14	
#15	1.25	3.50	575.00	3.60	1.93	101.73	2.67	5.92	115.90	51.53
	0.11	3.25	473.00	3.60	1.93	6.98	2.98	6.22	21.76	
	4.25	1.40	649.00	3.60	1.93	406.41	20.58	11.94	444.49	
#12	2.25	3.50	575.00	4.00	2.14	203.46	2.97	6.58	219.20	160.03
	1.11	3.25	473.00	4.00	2.14	78.32	3.31	6.91	94.72	
	5.25	1.40	649.00	4.00	2.14	557.81	22.86	13.26	600.13	
#16	3.25	3.50	575.00	4.40	2.36	323.28	3.26	7.24	340.58	174.60
	2.11	3.25	473.00	4.40	2.36	163.76	3.64	7.60	181.80	
	6.25	1.40	649.00	4.40	2.36	730.47	25.15	14.59	777.01	
#17	4.25	3.50	575.00	4.80	2.57	461.18	3.56	7.89	480.05	545.62
	3.11	3.25	473.00	4.80	2.57	263.31	3.97	8.29	282.99	
	7.25	1.40	649.00	4.80	2.57	924.38	27.43	15.92	975.14	
#25	1.25	3.50	575.00	4.20	2.25	118.68	3.12	6.91	135.20	129.56
	0.11	3.25	473.00	4.20	2.25	8.15	3.48	7.25	25.37	
	4.25	1.40	649.00	4.20	2.25	474.14	24.01	13.93	518.57	
#22	2.25	3.50	575.00	4.60	2.46	233.98	3.41	7.57	252.07	252.11
	1.11	3.25	473.00	4.60	2.46	90.06	3.81	7.94	108.92	
	5.25	1.40	649.00	4.60	2.46	641.48	26.29	15.25	690.14	
#26	3.25	3.50	575.00	5.00	2.68	367.36	3.71	8.22	387.02	197.69
	2.11	3.25	473.00	5.00	2.68	186.09	4.14	8.63	206.58	
	6.25	1.40	649.00	5.00	2.68	830.08	28.58	16.58	882.96	
#27	4.25	3.50	575.00	5.40	2.89	518.82	4.01	8.88	540.05	343.15
	3.11	3.25	473.00	5.40	2.89	296.22	4.47	9.33	318.36	
	7.25	1.40	649.00	5.40	2.89	1039.92	30.86	17.91	1097.03	
#1	2.25	4.50	575.00	4.20	2.25	213.63	2.20	5.85	228.19	350.82
	1.11	4.25	473.00	4.20	2.25	82.23	2.38	6.08	97.18	
	5.25	2.40	649.00	4.20	2.25	585.70	5.73	8.89	606.81	
#11	2.25	4.50	575.00	4.20	2.25	213.63	2.20	5.85	228.19	142.88
	1.11	4.25	473.00	4.20	2.25	82.23	2.38	6.08	97.18	
	5.25	2.40	649.00	4.20	2.25	585.70	5.73	8.89	606.81	
#21	2.25	4.50	575.00	4.80	2.57	244.15	2.52	6.69	260.78	224.24
	1.11	4.25	473.00	4.80	2.57	93.98	2.72	6.95	111.06	
	5.25	2.40	649.00	4.80	2.57	669.38	6.54	10.16	693.50	

Fig. 1.5 Specific on-resistance components (in $m\Omega.cm^2$) of 4H-SiC ACCUFETs on 10 μm thick epilayer at room temperature and at 200 °C.

At room temperature

Device	Lch (um)	Wjch (um)	tox (A)	Rcs	Rn+	Rchannel	Rjfet	Rdrift	Ron,estimated	Ron,measured
#1	2.25	4.50	695.00	7.00	17.64	21070.23	15.17	19.33	21129.42	10758.28
	1.11	4.25	566.00	7.00	17.64	6658.87	17.96	20.38	6721.90	
	5.25	3.60	740.00	7.00	17.64	38958.66	34.43	24.51	39042.28	
#11	2.25	4.50	695.00	7.00	17.64	21070.23	15.17	19.33	21129.42	10481.81
	1.11	4.25	566.00	7.00	17.64	6658.87	17.96	20.38	6721.90	
	5.25	3.60	740.00	7.00	17.64	38958.66	34.43	24.51	39042.28	
#21	2.25	4.50	695.00	8.00	20.16	24060.27	17.33	21.84	24147.65	7886.75
	1.11	4.25	566.00	8.00	20.16	7610.14	20.52	23.05	7681.92	
	5.25	3.60	740.00	8.00	20.16	44524.18	39.35	27.80	44619.53	

At 200 °C

Device	Lch (um)	Wjch (um)	tox (A)	Rcs	Rn+	Rchannel	Rjfet	Rdrift	Ron,estimated	Ron,measured
#1	2.25	4.50	695.00	4.20	10.50	1453.12	41.15	56.69	1565.70	1800.02
	1.11	4.25	566.00	4.20	10.50	476.97	48.07	59.56	599.35	
	5.25	3.60	740.00	4.20	10.50	2812.12	85.48	70.44	2982.78	
#11	2.25	4.50	695.00	4.20	10.50	1453.12	41.15	56.69	1565.70	1807.50
	1.11	4.25	566.00	4.20	10.50	476.97	48.07	59.56	599.35	
	5.25	3.60	740.00	4.20	10.50	2812.12	85.48	70.44	2982.78	
#21	2.25	4.50	695.00	4.80	12.00	1660.71	47.02	64.01	1788.59	1232.79
	1.11	4.25	566.00	4.80	12.00	545.10	54.94	67.33	684.21	
	5.25	3.60	740.00	4.80	12.00	3213.85	97.69	79.85	3408.23	

Fig. 1.6 Specific on-resistance components (in $m\Omega.cm^2$) of 4H-SiC ACCUFETs on 20 μm thick epilayer at room temperature and at 200 °C.

At room temperature

Device	Lch (um)	Wjch (um)	tox (A)	Rcs	Rn+	Rchannel	Rjfet	Rdrift	Ron,estimated	Ron,measured
#1	2.25	4.50	693.00	7.00	18.00	10956.52	8.45	17.45	11007.48	13858.73
	1.11	4.25	625.00	7.00	18.00	4386.97	9.66	18.09	4439.77	
	5.25	3.60	723.00	7.00	18.00	28048.03	15.40	20.35	28108.82	
#11	2.25	4.50	693.00	7.00	18.00	10956.52	8.45	17.45	11007.48	23425.60
	1.11	4.25	625.00	7.00	18.00	4386.97	9.66	18.09	4439.77	
	5.25	3.60	723.00	7.00	18.00	28048.03	15.40	20.35	28108.82	
#21	2.25	4.50	693.00	8.00	20.57	12521.74	9.66	19.26	12579.27	7618.08
	1.11	4.25	625.00	8.00	20.57	5013.68	11.05	19.99	5073.33	
	5.25	3.60	723.00	8.00	20.57	32054.89	17.59	22.60	32123.70	

At 200 °C

Device	Lch (um)	Wjch (um)	tox (A)	Rcs	Rn+	Rchannel	Rjfet	Rdrift	Ron,estimated	Ron,measured
#1	2.25	4.50	693.00	4.20	9.00	721.14	24.43	53.61	812.42	948.09
	1.11	4.25	625.00	4.20	9.00	306.18	27.73	55.47	402.62	
	5.25	3.60	723.00	4.20	9.00	1793.42	42.73	61.96	1911.36	
#11	2.25	4.50	693.00	4.20	9.00	721.14	24.43	53.61	812.42	1760.62
	1.11	4.25	625.00	4.20	9.00	306.18	27.73	55.47	402.62	
	5.25	3.60	723.00	4.20	9.00	1793.42	42.73	61.96	1911.36	
#21	2.25	4.50	693.00	4.80	10.28	824.16	27.92	59.09	926.30	560.96
	1.11	4.25	625.00	4.80	10.28	349.92	31.69	61.25	457.99	
	5.25	3.60	723.00	4.80	10.28	2049.62	48.84	68.74	2182.33	

Fig. 1.7 Specific on-resistance components (in $m\Omega.cm^2$) of 4H-SiC ACCUFETs on 30 μm thick epilayer at room temperature and at 200 °C.

At room temperature

Device	Lch (um)	Wjch (um)	tox (A)	Rcs	Rn+	Rchannel	Rjfet	Rdrift	Ron,estimated	Ron,measured
#5	1.25	3.50	610.00	6.00	19.44	3726.71	14.52	22.19	3788.90	9406.01
	0.11	3.25	500.00	6.00	19.44	223.20	19.39	23.41	291.48	
	4.25	2.60	693.00	6.00	19.44	17019.39	150.51	32.40	17227.78	
#2	2.25	3.50	610.00	6.67	21.60	7453.42	16.13	23.65	7521.51	10239.61
	1.11	3.25	500.00	6.67	21.60	2502.51	21.54	25.02	2577.38	
	5.25	2.60	693.00	6.67	21.60	23359.94	167.24	35.02	23590.51	
#6	3.25	3.50	610.00	7.33	23.76	11842.65	17.75	25.16	11916.70	22159.03
	2.11	3.25	500.00	7.33	23.76	5232.72	23.69	26.67	5314.23	
	6.25	2.60	693.00	7.33	23.76	30590.40	183.96	37.69	30843.19	
#7	4.25	3.50	610.00	8.00	25.92	16894.41	19.36	26.72	16974.45	29175.78
	3.11	3.25	500.00	8.00	25.92	8413.84	25.85	28.37	8502.03	
	7.25	2.60	693.00	8.00	25.92	38710.76	200.68	40.41	38985.82	
#15	1.25	3.50	610.00	6.00	19.44	3726.71	14.52	22.19	3788.90	5609.57
	0.11	3.25	500.00	6.00	19.44	223.20	19.39	23.41	291.48	
	4.25	2.60	693.00	6.00	19.44	17019.39	150.51	32.40	17227.78	
#12	2.25	3.50	610.00	6.67	21.60	7453.42	16.13	23.65	7521.51	7471.79
	1.11	3.25	500.00	6.67	21.60	2502.51	21.54	25.02	2577.38	
	5.25	2.60	693.00	6.67	21.60	23359.94	167.24	35.02	23590.51	
#16	3.25	3.50	610.00	7.33	23.76	11842.65	17.75	25.16	11916.70	13157.61
	2.11	3.25	500.00	7.33	23.76	5232.72	23.69	26.67	5314.23	
	6.25	2.60	693.00	7.33	23.76	30590.40	183.96	37.69	30843.19	
#17	4.25	3.50	610.00	8.00	25.92	16894.41	19.36	26.72	16974.45	21456.93
	3.11	3.25	500.00	8.00	25.92	8413.84	25.85	28.37	8502.03	
	7.25	2.60	693.00	8.00	25.92	38710.76	200.68	40.41	38985.82	
#25	1.25	3.50	610.00	7.00	22.68	4347.83	16.94	24.34	4418.83	5115.61
	0.11	3.25	500.00	7.00	22.68	260.40	22.62	25.77	338.51	
	4.25	2.60	693.00	7.00	22.68	19855.95	175.80	36.25	20097.53	
#22	2.25	3.50	610.00	7.67	24.84	8571.43	18.55	25.88	8648.41	4439.51
	1.11	3.25	500.00	7.67	24.84	2877.88	24.77	27.46	2962.66	
	5.25	2.60	693.00	7.67	24.84	26863.94	192.32	38.96	27127.77	
#26	3.25	3.50	610.00	8.33	27.00	13457.56	20.17	27.46	13540.57	7743.93
	2.11	3.25	500.00	8.33	27.00	5946.27	26.93	29.18	6037.76	
	6.25	2.60	693.00	8.33	27.00	34761.82	209.05	41.70	35047.95	
#27	4.25	3.50	610.00	9.00	29.16	19006.21	21.78	29.08	19095.28	11540.02
	3.11	3.25	500.00	9.00	29.16	9465.57	29.08	30.95	9563.80	
	7.25	2.60	693.00	9.00	29.16	43549.61	225.77	44.49	43858.07	
#1	2.25	4.50	610.00	7.00	22.68	7826.09	8.45	21.03	7885.29	13171.18
	1.11	4.25	500.00	7.00	22.68	2627.63	9.66	21.66	2688.68	
	5.25	3.60	693.00	7.00	22.68	24527.94	15.40	23.92	24596.98	
#11	2.25	4.50	610.00	7.00	22.68	7826.09	8.45	21.03	7885.29	12000.00
	1.11	4.25	500.00	7.00	22.68	2627.63	9.66	21.66	2688.68	
	5.25	3.60	693.00	7.00	22.68	24527.94	15.40	23.92	24596.98	
#21	2.25	4.50	610.00	8.00	25.92	8944.10	9.66	22.83	9010.55	3425.44
	1.11	4.25	500.00	8.00	25.92	3003.01	11.05	23.56	3071.58	
	5.25	3.60	693.00	8.00	25.92	28031.93	17.59	26.17	28109.66	

At 200 °C

Device	Lch (um)	Wch (um)	tox (A)	Rcs	Rn+	Rchannel	Rjfet	Rdrift	Ron,estimated	Ron,measured
#5	1.25	3.50	610.00	3.60	9.00	310.56	39.96	67.77	430.93	1945.90
	0.11	3.25	500.00	3.60	9.00	19.65	51.69	71.15	155.13	
	4.25	2.60	693.00	3.60	9.00	1341.55	218.68	90.66	1663.54	
#2	2.25	3.50	610.00	4.00	10.00	621.12	44.40	72.16	751.72	1876.35
	1.11	3.25	500.00	4.00	10.00	220.27	57.43	75.94	367.69	
	5.25	2.60	693.00	4.00	10.00	1841.34	242.98	97.68	2196.05	
#6	3.25	3.50	610.00	4.40	11.00	986.89	48.84	76.71	1127.88	2364.97
	2.11	3.25	500.00	4.40	11.00	460.58	63.18	80.89	620.09	
	6.25	2.60	693.00	4.40	11.00	2411.28	267.28	104.86	2798.86	
#7	4.25	3.50	610.00	4.80	12.00	1407.87	53.27	81.40	1559.39	2559.51
	3.11	3.25	500.00	4.80	12.00	740.58	68.92	85.97	912.32	
	7.25	2.60	693.00	4.80	12.00	3051.36	291.58	112.17	3471.95	
#15	1.25	3.50	610.00	3.60	9.00	310.56	39.96	67.77	430.93	1530.26
	0.11	3.25	500.00	3.60	9.00	19.65	51.69	71.15	155.13	
	4.25	2.60	693.00	3.60	9.00	1341.55	218.68	90.66	1663.54	
#12	2.25	3.50	610.00	4.00	10.00	621.12	44.40	72.16	751.72	1719.20
	1.11	3.25	500.00	4.00	10.00	220.27	57.43	75.94	367.69	
	5.25	2.60	693.00	4.00	10.00	1841.34	242.98	97.68	2196.05	
#16	3.25	3.50	610.00	4.40	11.00	986.89	48.84	76.71	1127.88	2232.64
	2.11	3.25	500.00	4.40	11.00	460.58	63.18	80.89	620.09	
	6.25	2.60	693.00	4.40	11.00	2411.28	267.28	104.86	2798.86	
#17	4.25	3.50	610.00	4.80	12.00	1407.87	53.27	81.40	1559.39	2788.49
	3.11	3.25	500.00	4.80	12.00	740.58	68.92	85.97	912.32	
	7.25	2.60	693.00	4.80	12.00	3051.36	291.58	112.17	3471.95	
#25	1.25	3.50	610.00	4.20	10.50	362.32	46.62	74.23	497.91	1398.37
	0.11	3.25	500.00	4.20	10.50	22.92	60.31	78.18	176.15	
	4.25	2.60	693.00	4.20	10.50	1565.14	255.13	100.95	1935.96	
#22	2.25	3.50	610.00	4.60	11.50	714.29	51.06	78.87	860.36	1381.76
	1.11	3.25	500.00	4.60	11.50	253.31	66.05	83.22	418.72	
	5.25	2.60	693.00	4.60	11.50	2117.54	279.43	108.22	2521.33	
#26	3.25	3.50	610.00	5.00	12.50	1121.46	55.49	83.64	1278.15	2013.29
	2.11	3.25	500.00	5.00	12.50	523.39	71.79	88.39	701.11	
	6.25	2.60	693.00	5.00	12.50	2740.09	303.72	115.63	3176.98	
#27	4.25	3.50	610.00	5.40	13.50	1583.85	59.93	88.53	1751.26	2037.21
	3.11	3.25	500.00	5.40	13.50	833.15	77.54	93.68	1023.31	
	7.25	2.60	693.00	5.40	13.50	3432.78	328.02	123.15	3902.90	
#1	2.25	4.50	610.00	4.20	10.50	652.17	24.43	64.72	756.07	1228.20
	1.11	4.25	500.00	4.20	10.50	231.28	27.73	66.58	340.33	
	5.25	3.60	693.00	4.20	10.50	1933.41	42.73	73.07	2063.96	
#11	2.25	4.50	610.00	4.20	10.50	652.17	24.43	64.72	756.07	1224.94
	1.11	4.25	500.00	4.20	10.50	231.28	27.73	66.58	340.33	
	5.25	3.60	693.00	4.20	10.50	1933.41	42.73	73.07	2063.96	
#21	2.25	4.50	610.00	4.80	12.00	745.34	27.92	70.21	860.31	871.00
	1.11	4.25	500.00	4.80	12.00	264.32	31.69	72.36	385.22	
	5.25	3.60	693.00	4.80	12.00	2209.61	48.84	79.85	2355.14	

Fig. 1.8 Specific on-resistance components (in $m\Omega.cm^2$) of 4H-SiC ACCUFETs on 40 μm thick epilayer at room temperature and at 200 °C.

thicker epilayers is done using a different technique than the 10 μm epilayer. The surface roughness of the thicker epilayers is expected to be larger due to propagation of defects to surface, which can result in the lower mobilities. As described earlier, the small effective mobility values are due to a high density of interface traps. Similarly, the large threshold voltage is due a large effective negative oxide charge caused by the electrons in these traps. Hence, in order to obtain a low channel resistance, it is important to improve the technology to obtain higher quality SiO_2/SiC interfaces.

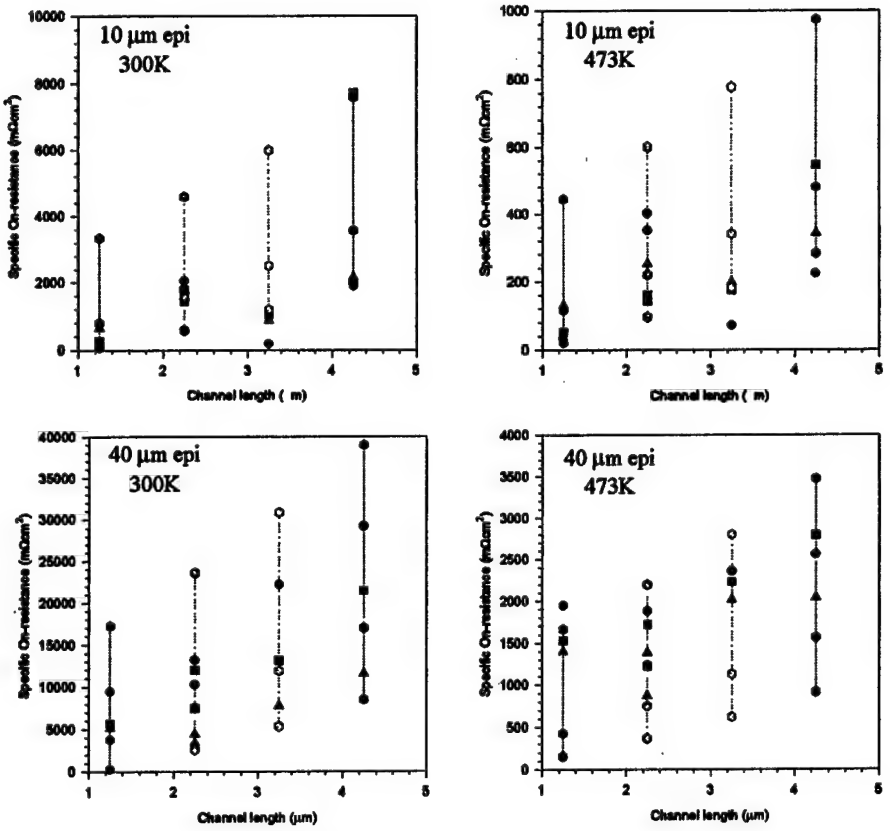

Fig. 1.9 Specific on-resistance dependence on channel length for different epilayers at room temperature and at 200 °C. (the measured values are represented by the dark symbols, and the estimated ranges are represented by the dotted lines and the light symbols enclosing them)

The contact specific resistance is about 6-8 $m\Omega.cm^2$ in all devices at room temperature and reduces to about 3.6-4.8 $m\Omega.cm^2$ at 200 °C. This contact resistance is not negligible compared to other resistance components, except the channel resistance which is huge. This indicates that although the contact resistance has been significantly reduced by choosing appropriate metals for the contact and by doing post-metallization anneals, there is further scope for improvement, and further studies could be done for obtaining very low resistance ohmic contacts to silicon carbide.

The N+ source resistance was about 20 $m\Omega.cm^2$ on most devices at room temperature, and reduced to approximately 10 $m\Omega.cm^2$ at the higher temperature. The large N+ source resistance is due to a large sheet resistance of the nitrogen implanted N+ source regions. The reduction in this resistance at higher temperature is caused by increased ionization of the dopants.

The JFET region resistance and the drift region resistance are of the same order of magnitude and both increase with temperature as shown in these figures. Both the JFET region and the drift region resistance depend on the JFET width, and hence, their estimates vary considerably between the three cases described above.

The dependence of the specific on-resistance of the ACCUFETs on the channel length is illustrated in Fig. 1.63. Due to the dominance of the channel resistance in the devices, the on-resistance also varies linearly with the channel length. It can be seen that the measured on-resistance of most devices (represented by the dark symbols in Fig. 1.63) falls in the estimated range that is represented by light symbols and dotted lines. In some cases, the on-resistance is lower than the estimates, which is probably due to higher mobilities in those regions.

		Designs 1 & 2				Design 3		
S. No.	Device Name	Lch (μm)	Gate Fingers	Wch (mm)	Wch/Lch	Gate Fingers	Wch (mm)	Wch/Lch
1	rmos211	2.25	9.0	2.70	1200	8.0	2.40	1067
2	rmos201	2.25	9.5	2.85	1267	8.0	2.40	1067
3	rmos191	2.25	10	3.00	1334	8.5	2.55	1133
4	rmos181	2.25	10.5	3.15	1400	9.0	2.70	1200
5	rmos182	1.25	10.5	3.15	2520	9.0	2.70	2160
6	rmos221	3.25	8.5	2.55	785	7.5	2.25	692
7	rmos241	4.25	8.0	2.40	565	7.0	2.10	494
8	rmos101	2.0	19.5	5.85	2925			
9	rmos242	3.25	8.0	2.40	738			
10	rmos262	3.25	7.0	2.10	646			

Wch (mm) = Channel Width = Gate Fingers * 2 * 0.15 (mm)
Lch (μm) = Channel Length

Fig. 1.10 Channel W/L ratios for different ACCUFET designs.

1.5.3 Saturation current

The saturation current per channel width is given by

$$\frac{I_{DS}}{Z} = \frac{\mu_{ns} C_{ox}}{2L}(V_G - V_T)^2 \qquad (1.5)$$

The saturation currents per unit channel width at a gate bias of 32 V were recorded and compared against the expected values from the model for selected ACCUFETs on 10 μm and 40 μm thick epilayers as discussed in the previous section.

The channel widths for the different ACCUFETs are listed in Fig. 1.64. The dependence of the measured saturation currents on the channel length is illustrated in Fig. 1.65. A range for the measured values based on process induced variations was estimated and is shown using light symbols and dotted lines. The saturation currents are found to vary inversely with channel length as expected from the model.

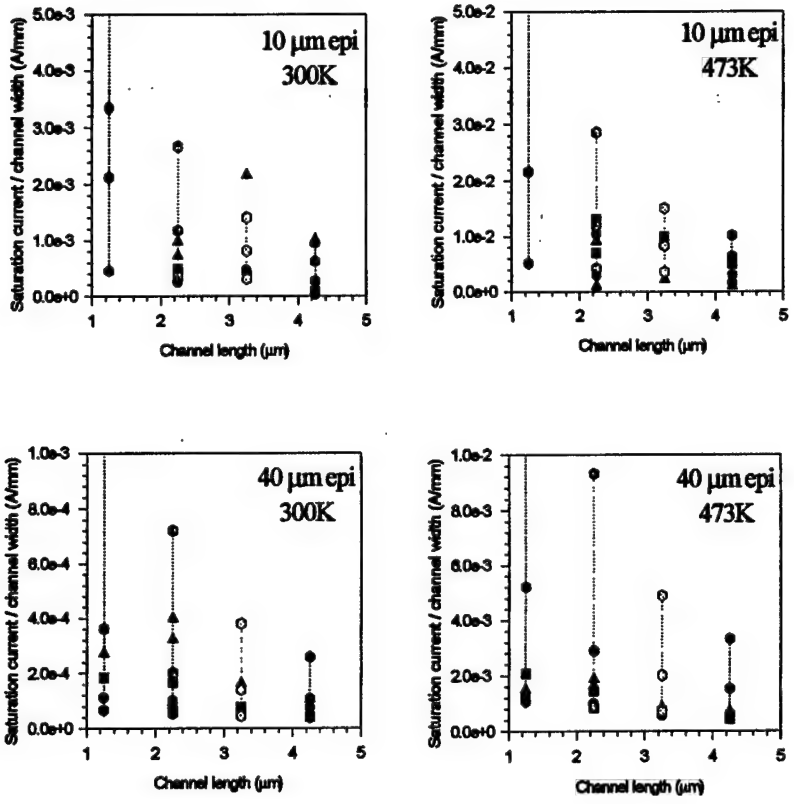

Fig. 1.11 Saturation current dependence on channel length for different epilayers. (the measured values are represented by the dark symbols, and the estimated ranges are represented by the dotted lines and the light symbols enclosing them)

1.5.4 Transconductance

The transconductance per channel width is given by

$$\frac{g_{ms}}{Z} = \frac{\mu_{ns} C_{ox}}{L}(V_G - V_T) \qquad (1.6)$$

The transconductance values per unit channel width at a gate bias of 32 V were recorded and compared against the expected values from the model for selected ACCUFETs on 10 µm and 40 µm thick epilayers as discussed earlier. A range for the measured values based on process induced variations was estimated. The dependence of the measured transconductance on the channel length is illustrated in Fig. 1.66. The

transconductance values also vary inversely with channel length as expected from the model.

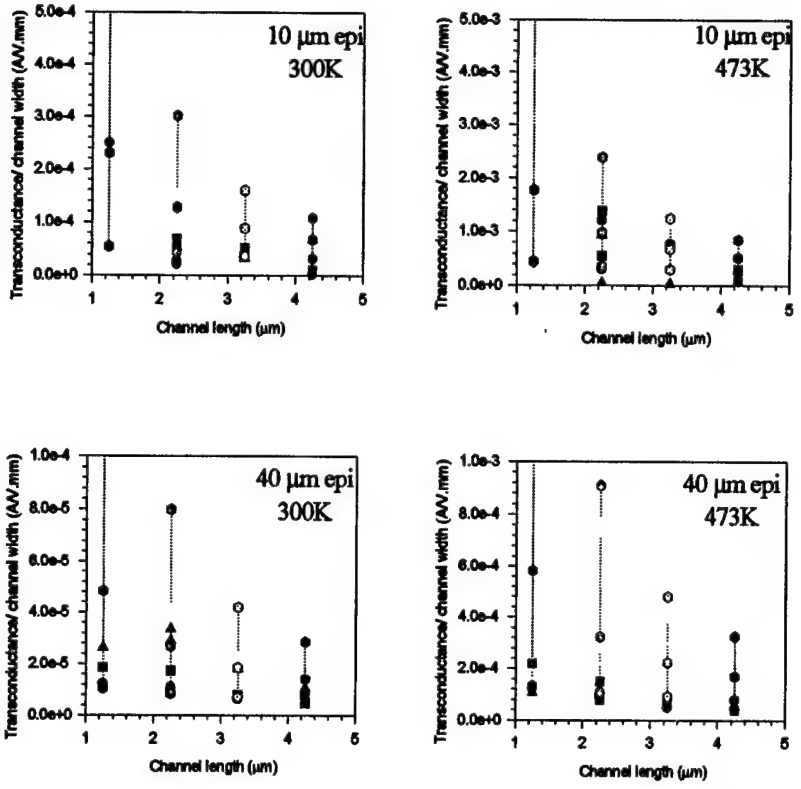

Fig. 1.12 Transconductance dependence on channel length for different epilayers. (the measured values are represented by the dark symbols, and the estimated ranges are represented by the dotted lines and the light symbols enclosing them)

1.6 Parasitic JFET regions

The ACCUFET contains two parasitic JFET regions: one is at the surface near the MOS channel and the other is between the buried P+ layers [2]. The *surface* JFET is designed to be pinched off at zero gate bias for an optimally designed ACCUFET structure. However, that may not be the case if (1) the doping of the buried P+ layer is not sufficiently high; (2) the doping of the N- region between the buried P+ layer and the gate is high, and (3) the thickness of the N- region between the buried P+ layer and the gate is large. Under these circumstances, there is current flow from the drain to the source through this surface JFET even at a zero gate bias. However, this current can be suppressed by independently applying a negative voltage to the buried P+ region. The current through the surface JFET was observed in some ACCUFETs on the 10 µm epilayer which had a doping of $1x10^{16}$ cm^{-3}. It was found that suppression of this current was possible by application of a negative bias to the P+ region as illustrated in Fig. 1.67.

Here, the source and the gate bias are maintained at zero, and the bias to the buried P+ layer was varied from 0V to -5V.

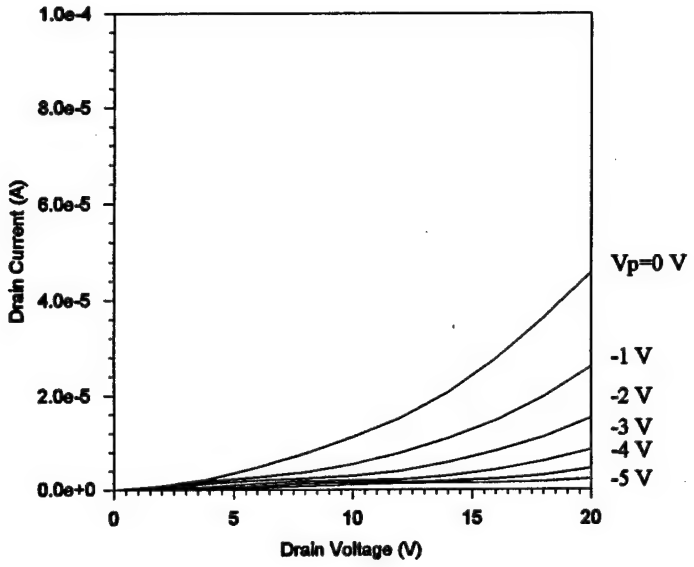

Fig. 1.13 Suppression of leakage through the surface JFET at zero gate bias by applying a negative bias to the buried P+ layer in an ACCUFET on a 10 μm epilayer with a doping of $1x10^{16}$ cm^{-3}. (L_{ch}=3.25 μm, W_{jch}=3.5 μm)

The *buried* JFET region is not expected to be pinched off at low drain voltages during the normal operation of the ACCUFET. However, that may not be the case if the doping of the N- region under the gate is low and/or if the width of the buried JFET region is small. Under these circumstances, the device shows triodelike characteristics with a significant offset drain voltage as explained earlier . However, this offset voltage can be reduced by independently applying a positive voltage to the buried P+ region. A large offset voltage due to the buried JFET was observed in some ACCUFETs on the 40 μm epilayer which had a low doping of $2x10^{15}$ cm^{-3}. The reduction of the offset voltage by application of a positive voltage to the P+ region is illustrated in Fig. 1.68. Here, the source and the gate bias are maintained at zero and 32 V, respectively, and the bias to the buried P+ layer was varied from -2 V to +5 V. The effects of the parasitic JFETs on the ACCUFETs are important to understand for designing ACCUFETs. Both the effects discussed in this section must be avoided by a careful design of the ACCUFET structure and the process.

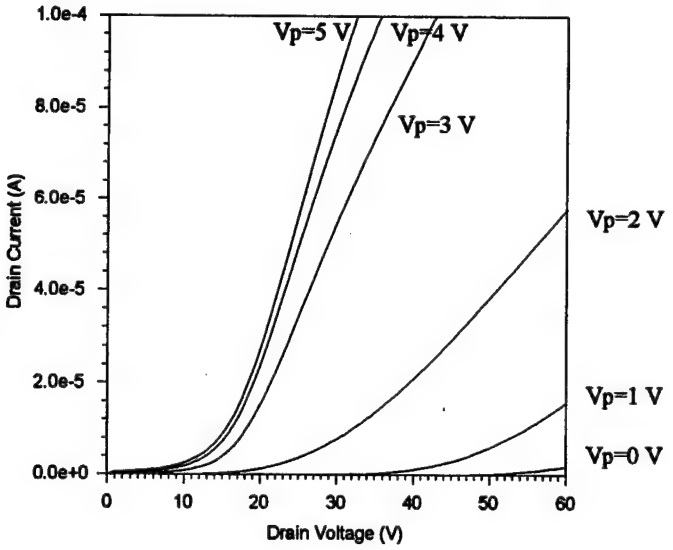

Fig. 1.14 Reduction in the offset voltage at a gate bias of 32 V by applying a positive bias to the buried P+ region in an ACCUFET on a 40 μm epilayer with a doping of $2x10^{15}$ cm^{-3}. (L_{ch}=2.25 μm, W_{jch}=1.5 μm)

1.7 References

1. R.K. Chilukuri and B.J. Baliga, "Fabrication of High Voltage 4H-SiC ACCUFETs," *PSRC Technical Report*, 2000.
2. R.K. Chilukuri and B.J. Baliga, "Analysis of High Voltage 4H-SiC ACCUFET Operation," *PSRC Technical Report*, 2000.
3. R. Schorner, P. Friedrichs, and D. Peters, *IEEE Trans. Electron Dev.*, vol. 46, pp. 533, March 1999.
4. D.M. Brown, et al., "SiC MOS Interface Characteristics," *IEEE Trans. Electron Dev.*, vol. 41, no. 4, pp. 618-620, April 1999.
5. N.S. Saks, S.S. Mani, A.K. Agarwal, and V.S. Hegde, "Hall mobility of inversion layers in 6H-SiC MOSFETs," Proceedings of ICSCRM, pp. 69, 1999.
6. N. Thapar and B.J. Baliga, "Analytical model for the threshold voltage of accumulation channel MOS-gate devices," *Solid-State Electronics*, vol. 42, no. 11, pp. 1975-1979, 1998.
7. W.J. Schaffer, et al., "Conductivity anisotropy in epitaxial 6H and 4H-SiC."

APPENDIX

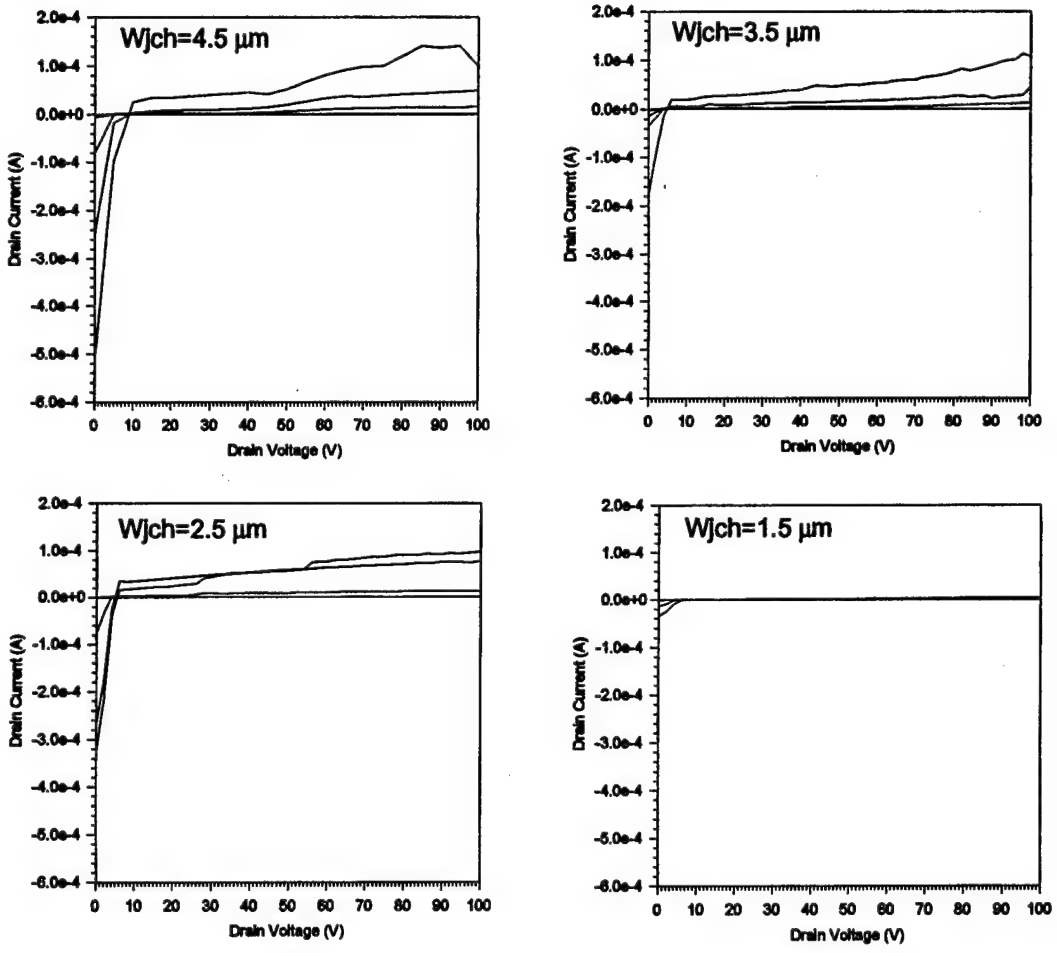

Fig. 1.1 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 1 on a 40 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (Thermal gate oxide,L_{ch}=2.25 µm)

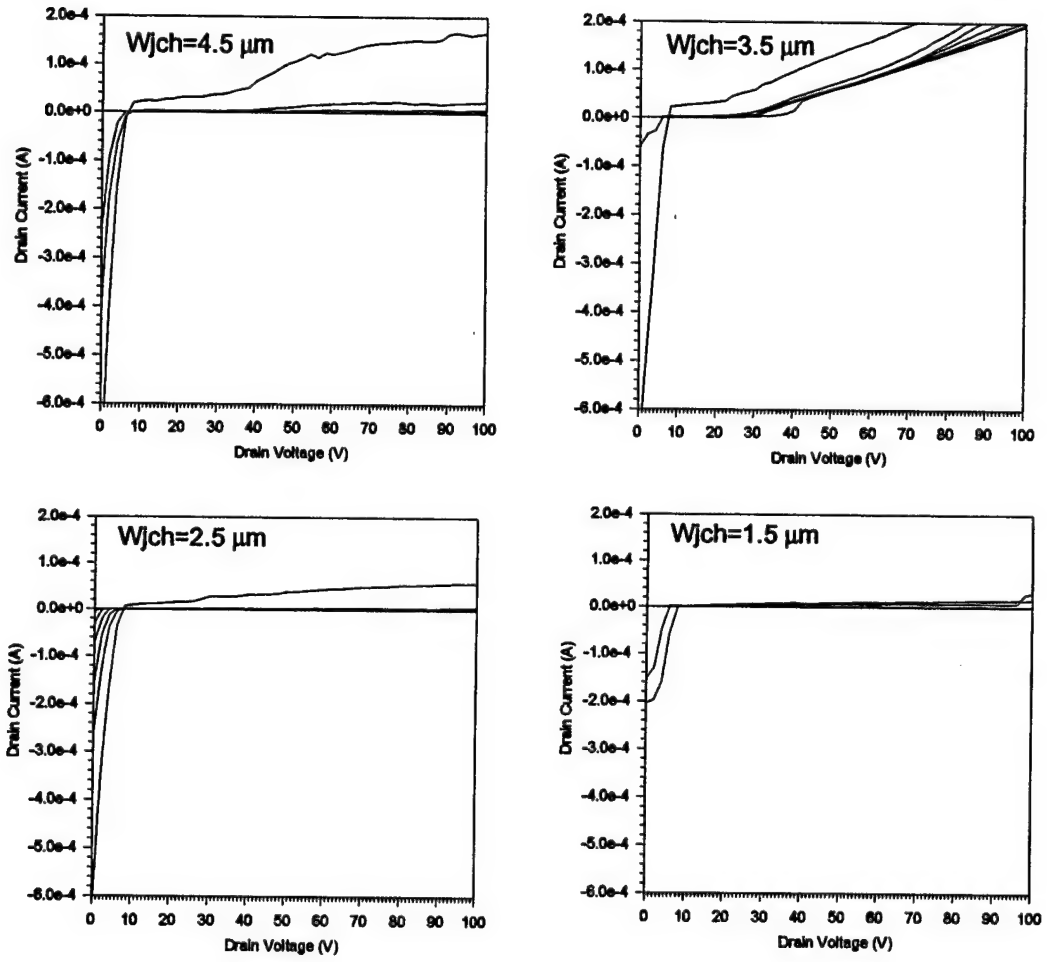

Fig. 1.2 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 2 on a 40 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (Thermal gate oxide,L_{ch}=2.25 µm)

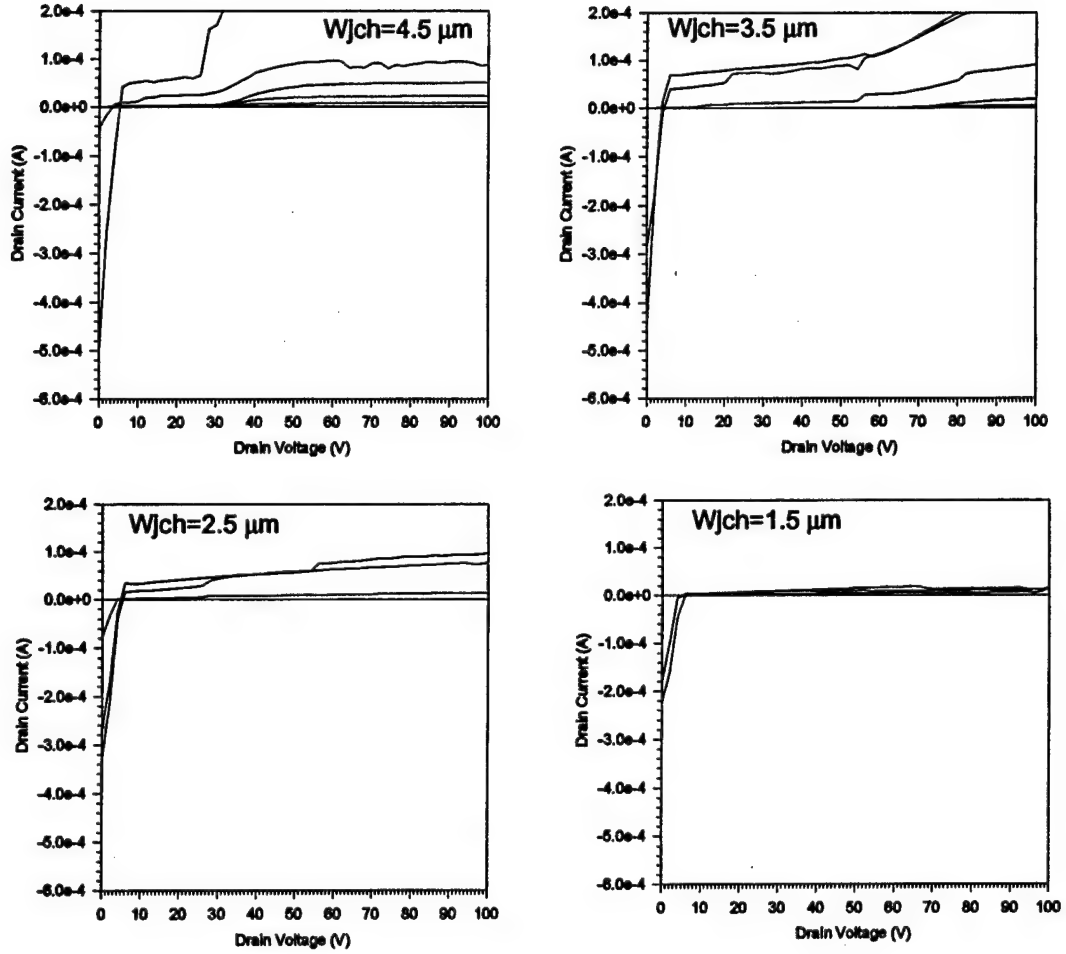

Fig. 1.3 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 3 on a 40 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (Thermal gate oxide,L_{ch}=2.25 µm)

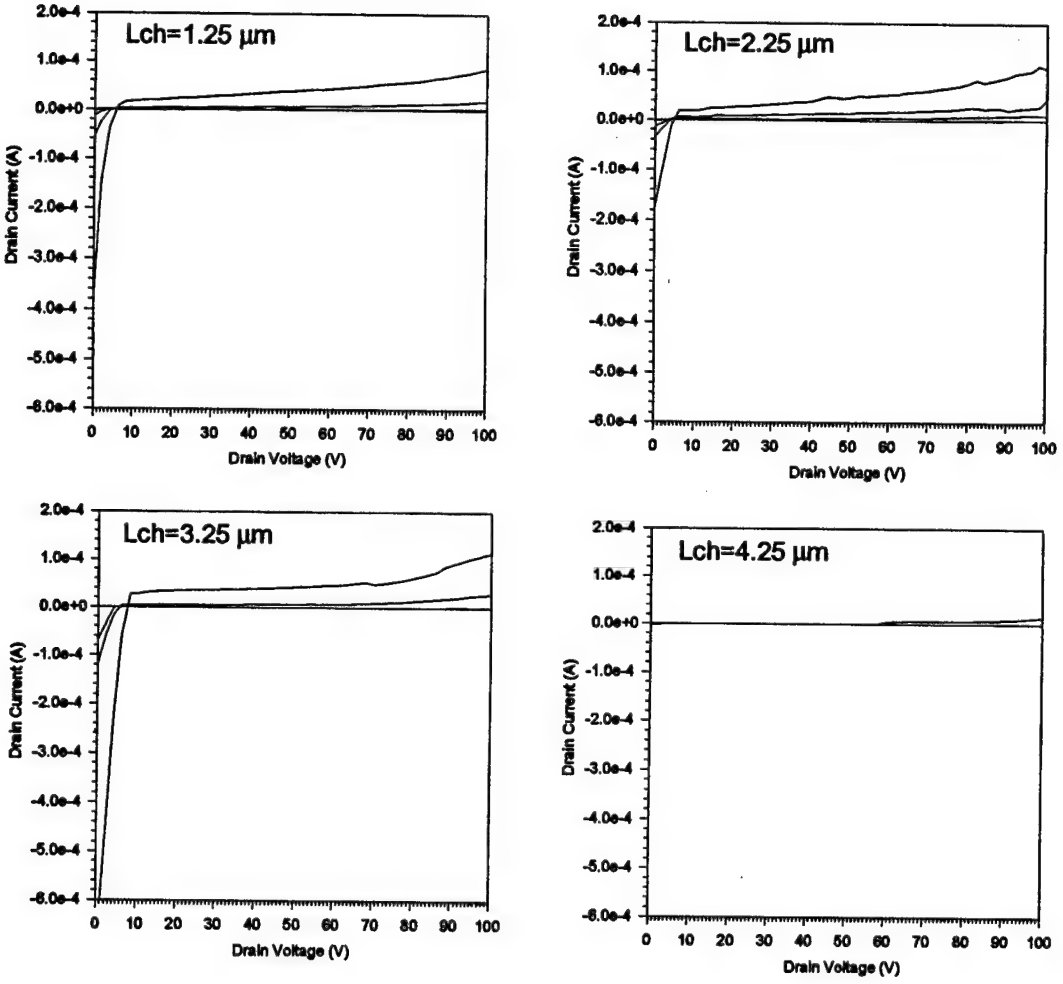

Fig. 1.4 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 1 on a 40 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (Thermal gate oxide, W_{jch}=3.5 µm)

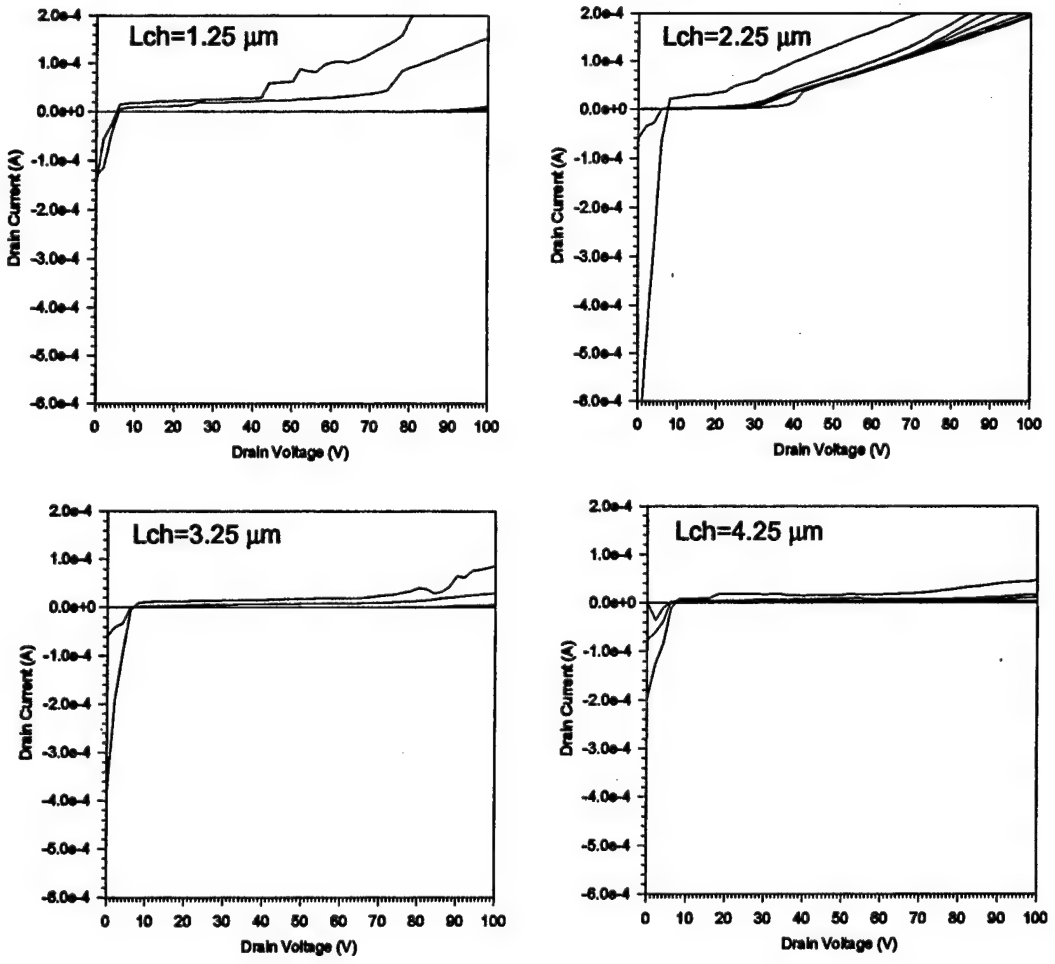

Fig. 1.5 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 2 on a 40 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (Thermal gate oxide, W_{jch}=3.5 µm)

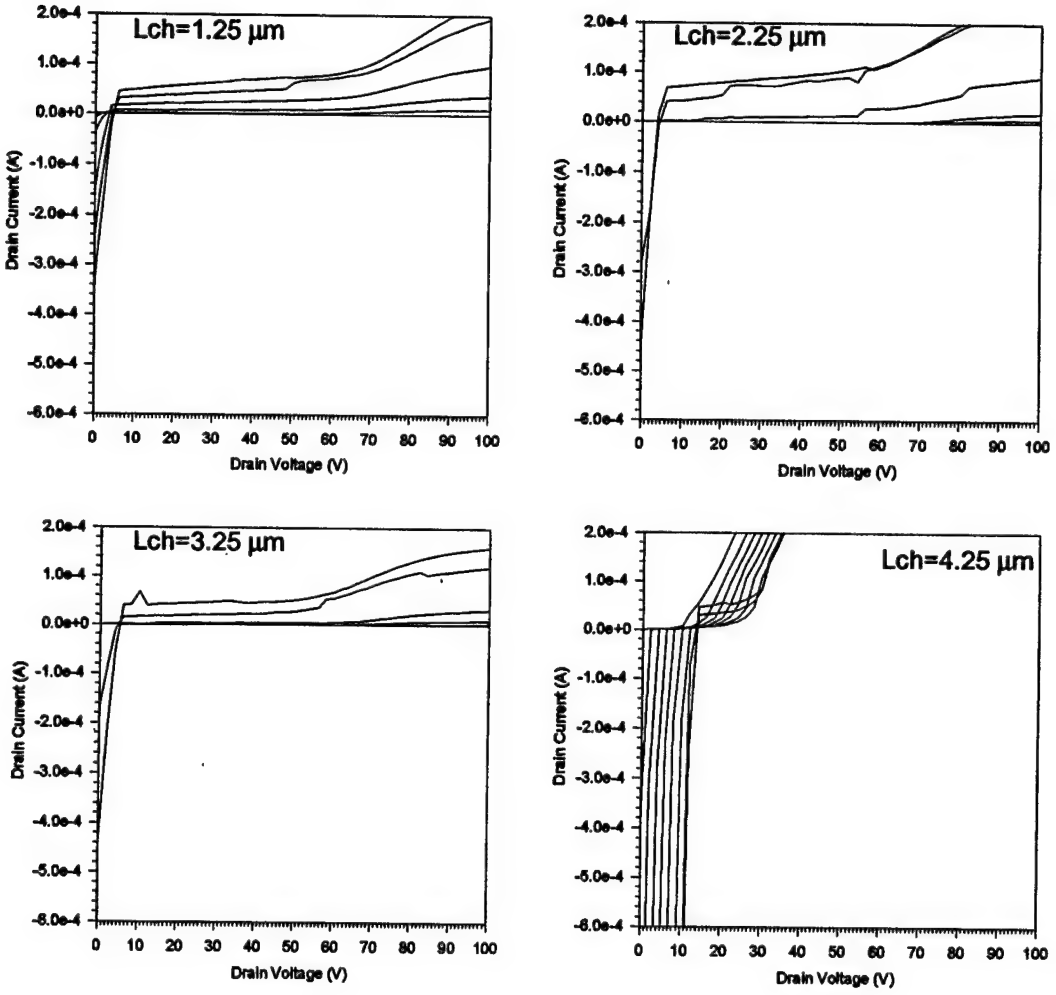

Fig. 1.6 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 3 on a 40 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (Thermal gate oxide, W_{jch}=3.5 µm)

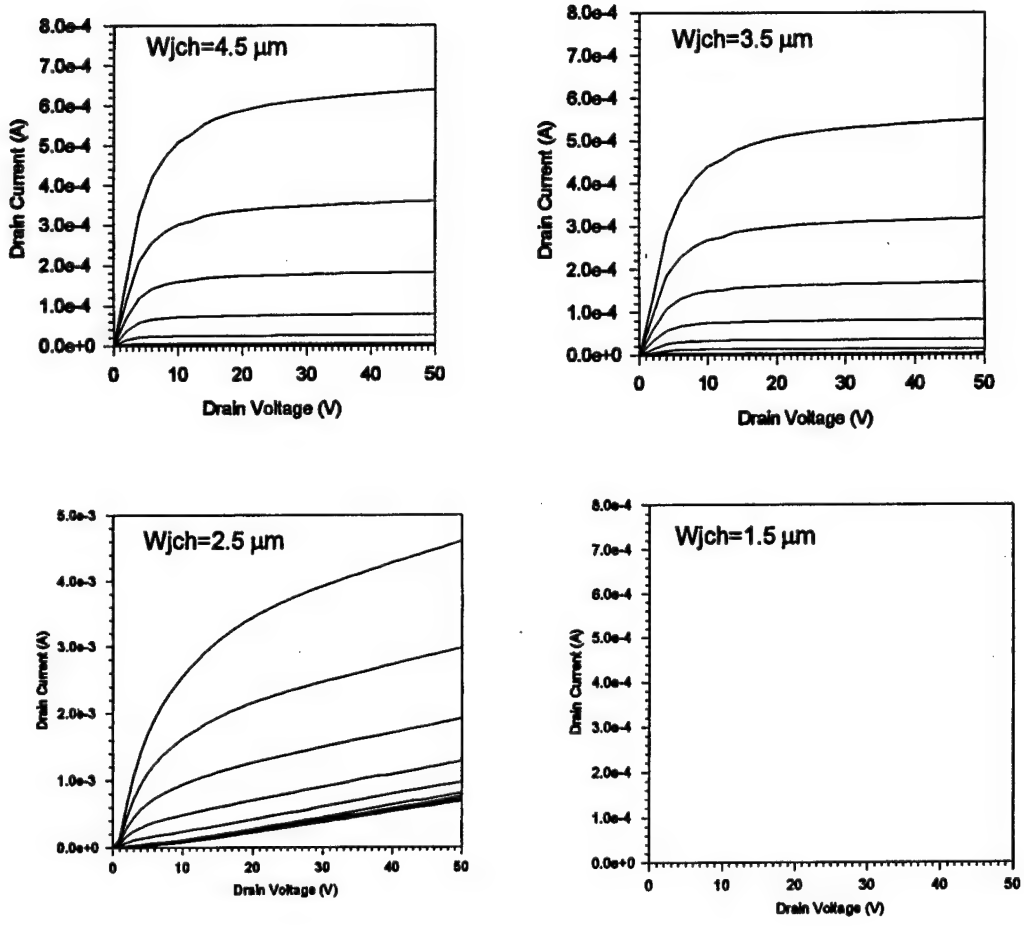

Fig. 1.7 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 1 on a 10 µm thick epilayer with a doping of $1x10^{16}$ cm^{-3} at room temperature (gate voltage varied from 0 to 50 V in steps of 5 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

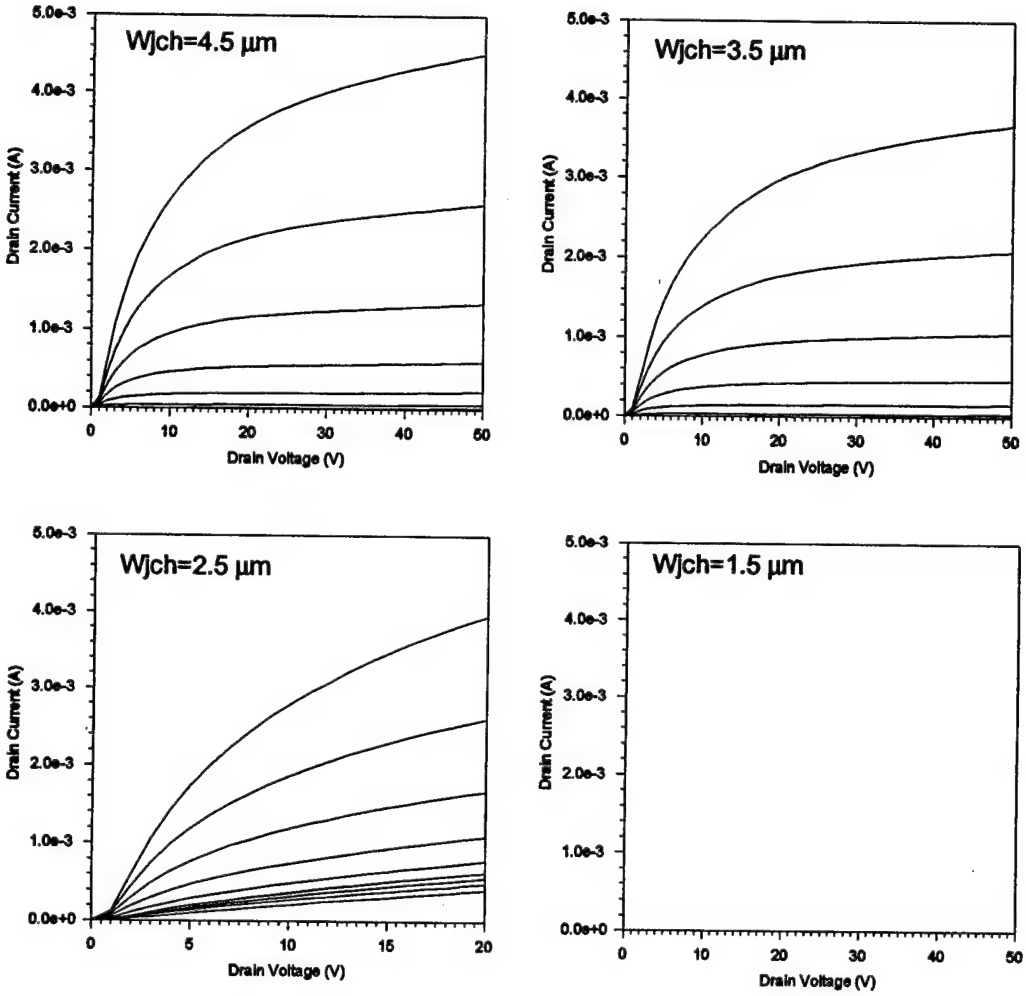

Fig. 1.8 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 2 on a 10 µm thick epilayer with a doping of $1x10^{16}$ cm^{-3} at room temperature (gate voltage varied from 0 to 50 V in steps of 5 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

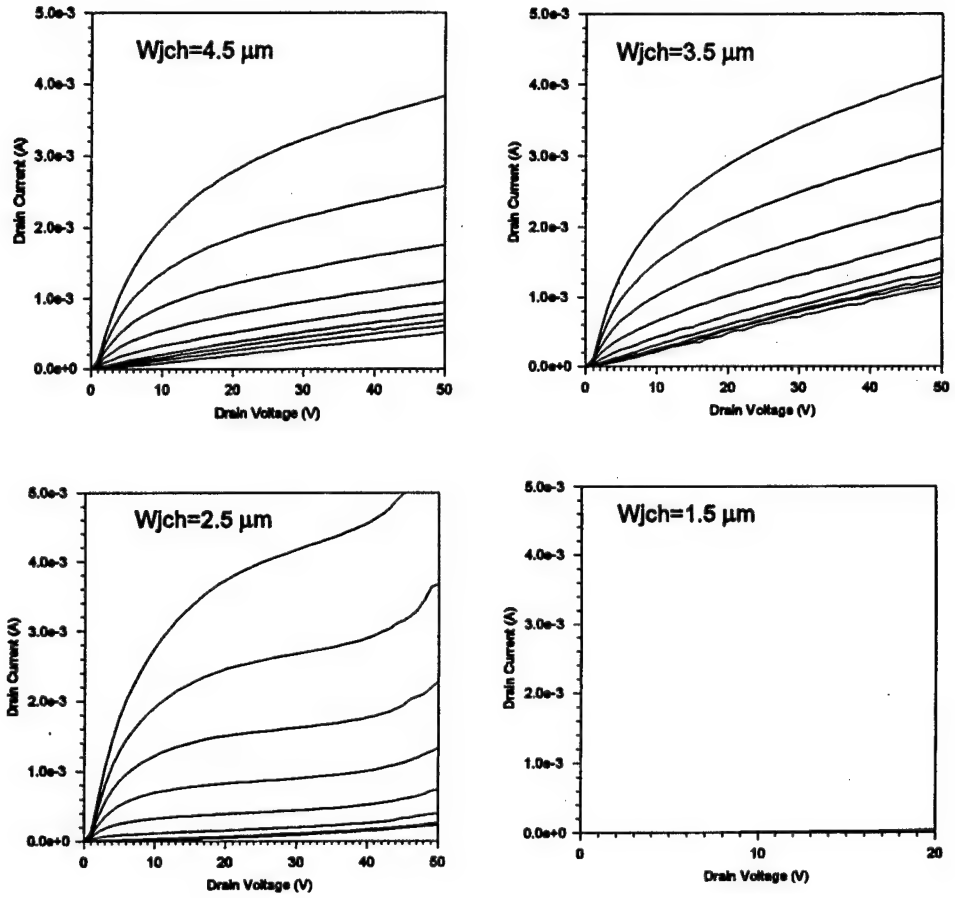

Fig. 1.9 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 3 on a 10 µm thick epilayer with a doping of $1x10^{16}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

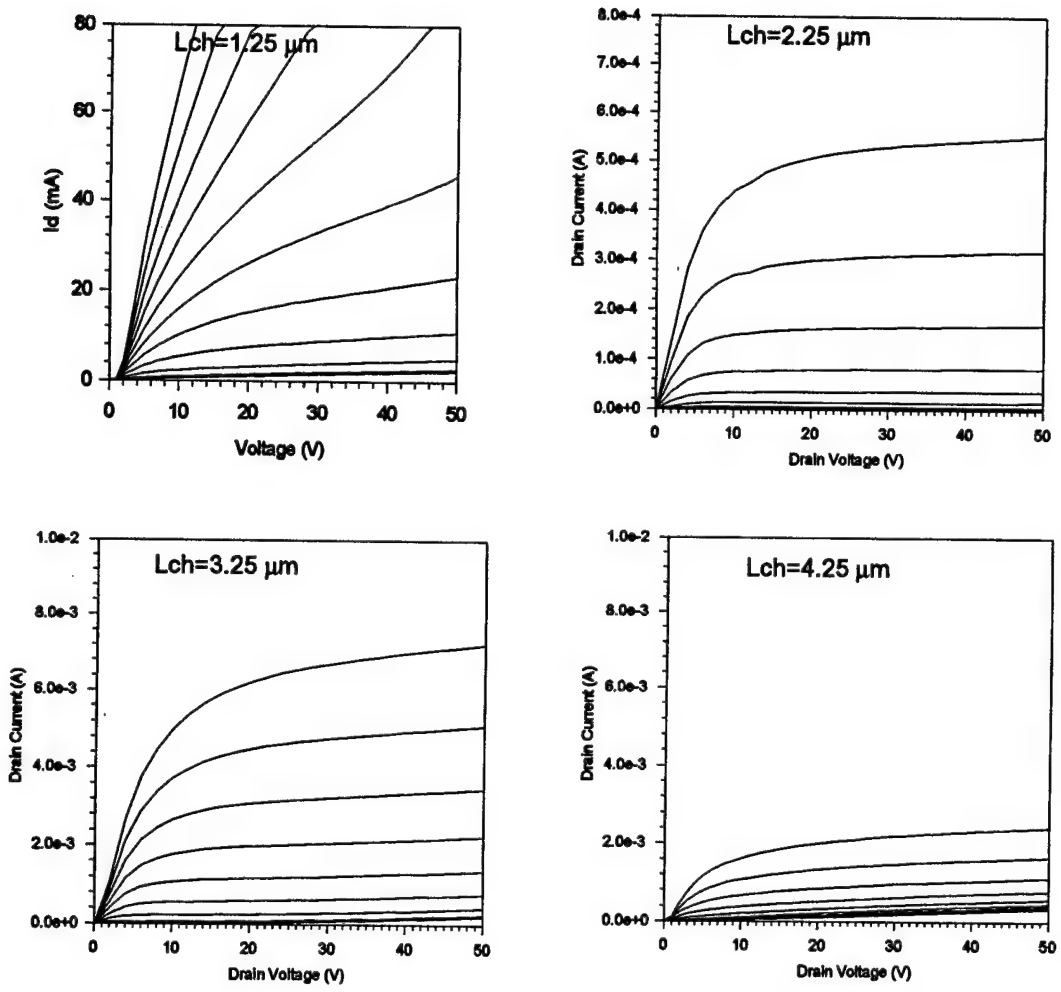

Fig. 1.10 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 1 on a 10 µm thick epilayer with a doping of $1x10^{16}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

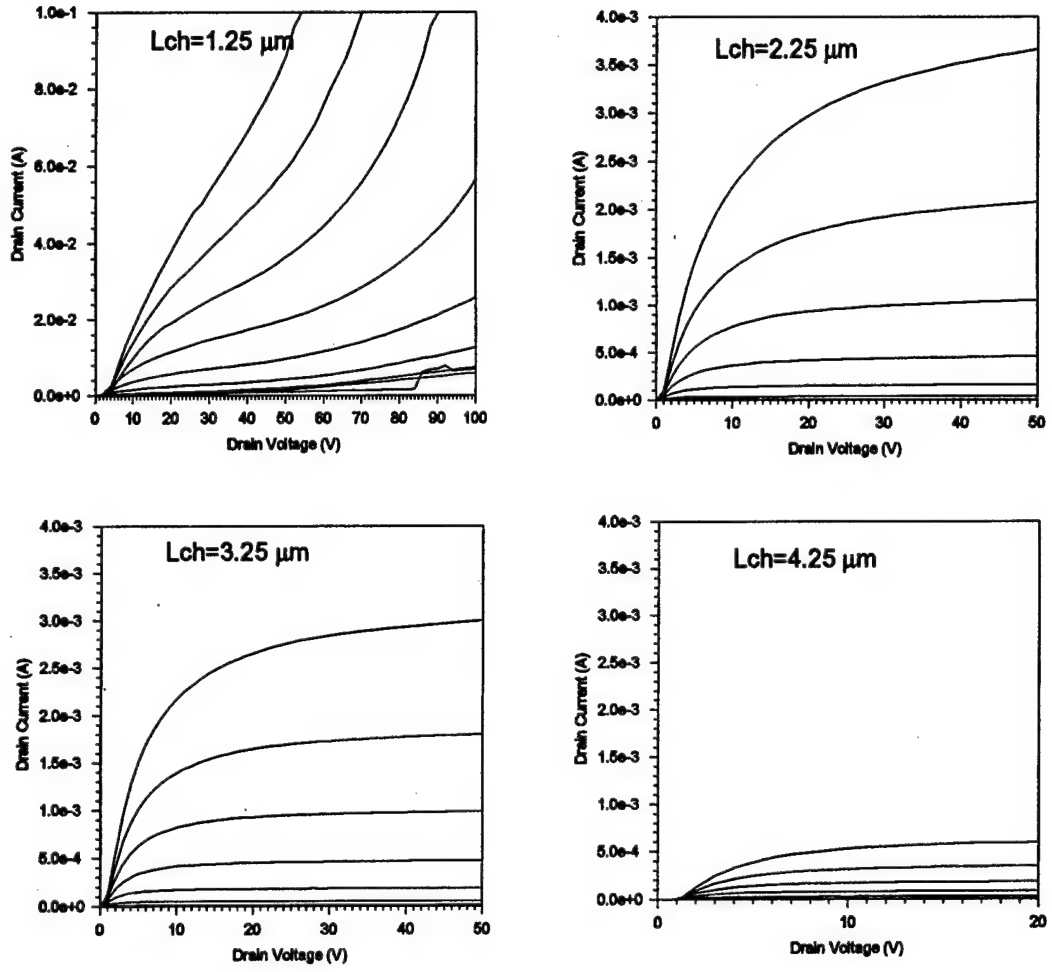

Fig. 1.11 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 2 on a 10 µm thick epilayer with a doping of $1x10^{16}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

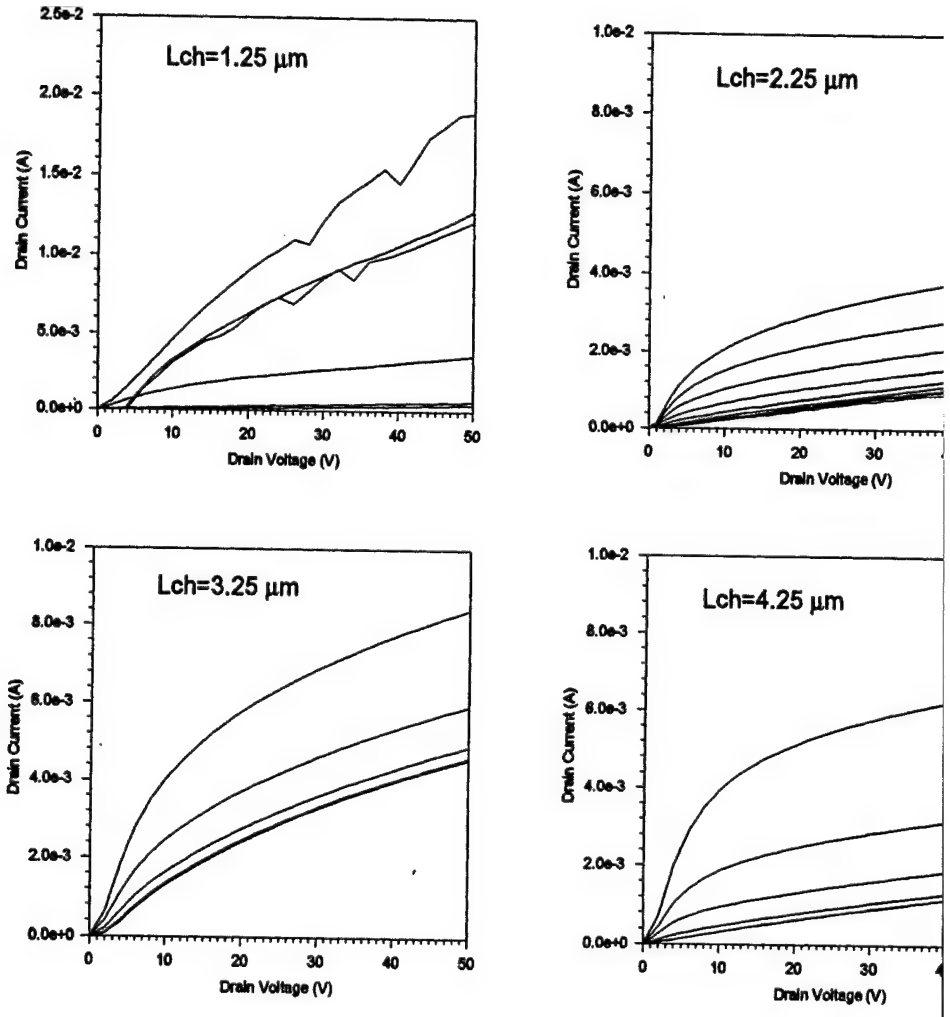

Fig. 1.12 Effect of the channel length (L_{ch}) on the output character ACCUFET of device structure 3 on a 10 µm thick epilayer w of $1x10^{16}$ cm^{-3} at room temperature (gate voltage varied from steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

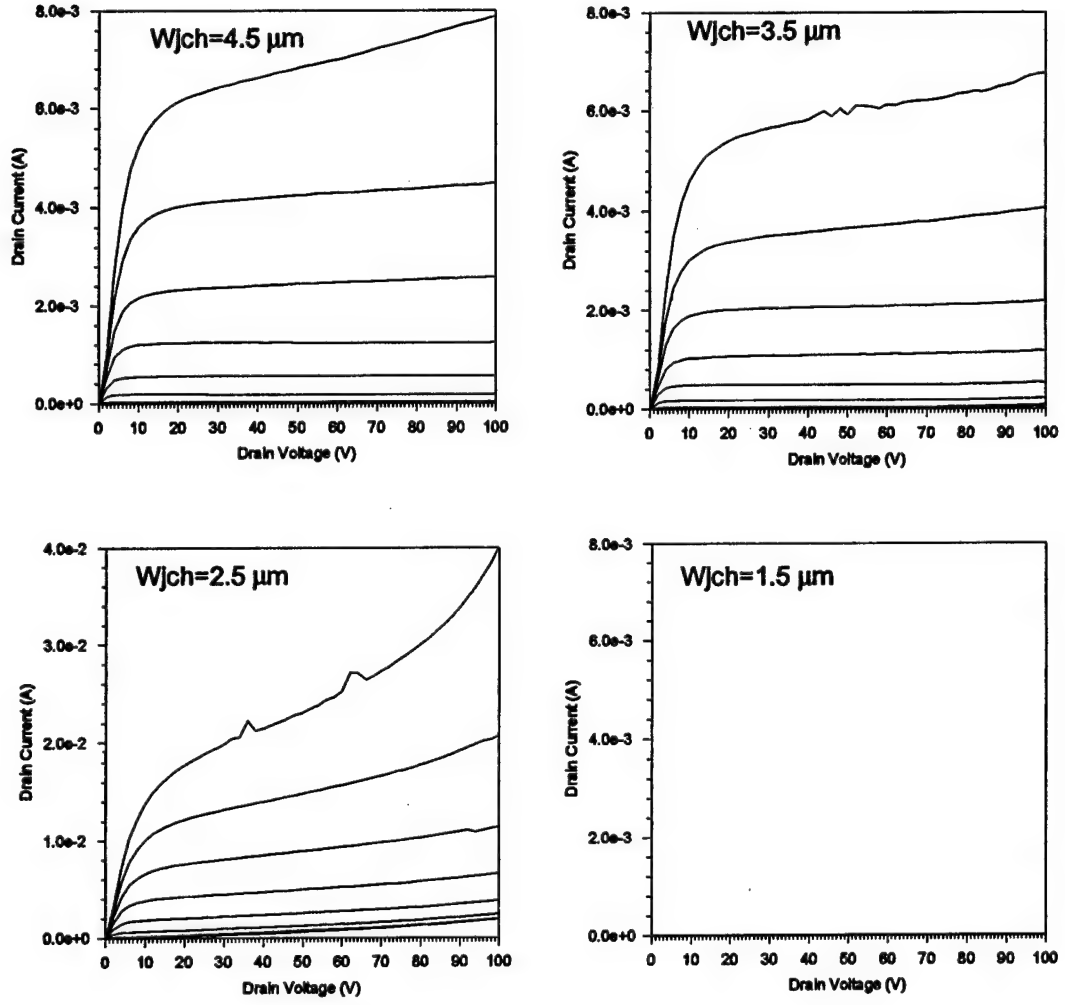

Fig. 1.13 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 1 on a 10 µm thick epilayer with a doping of $1x10^{16}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

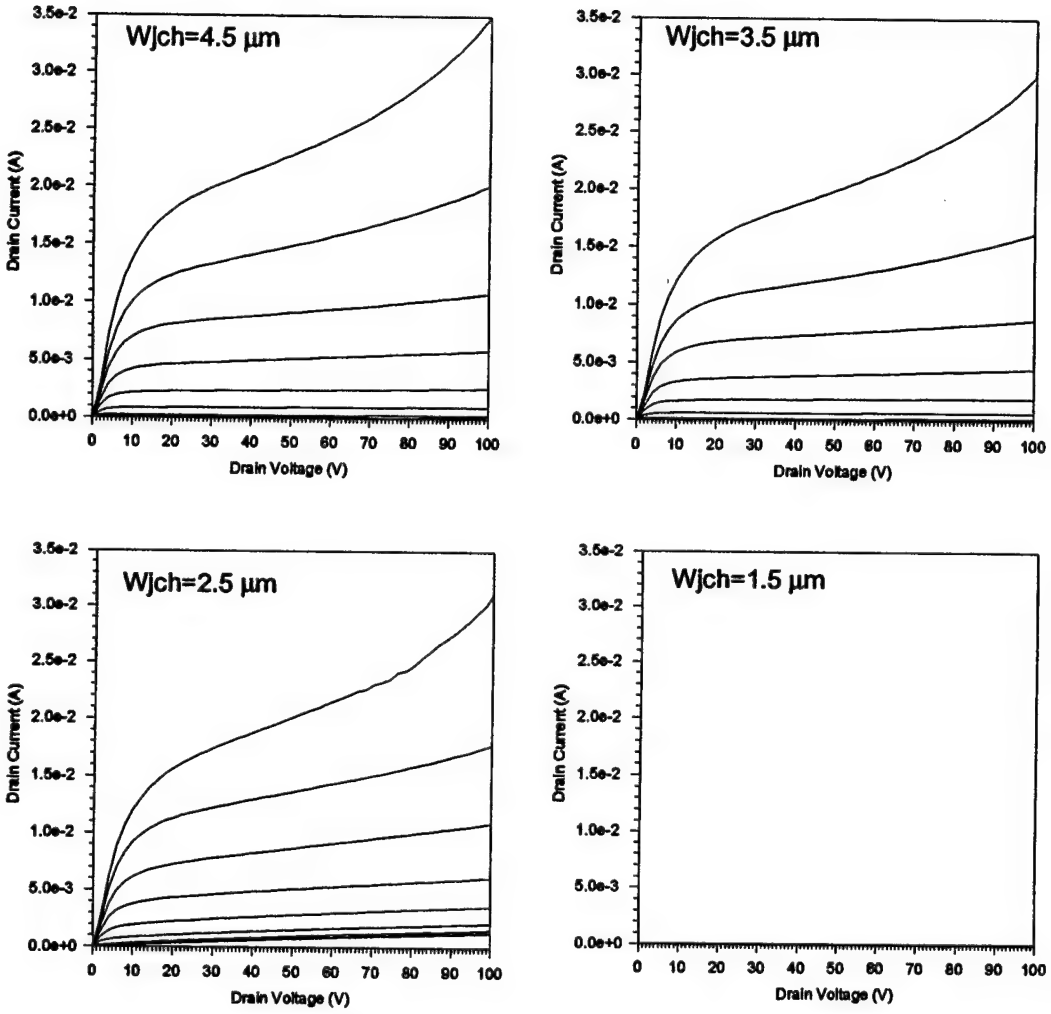

Fig. 1.14 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 2 on a 10 µm thick epilayer with a doping of $1x10^{16}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

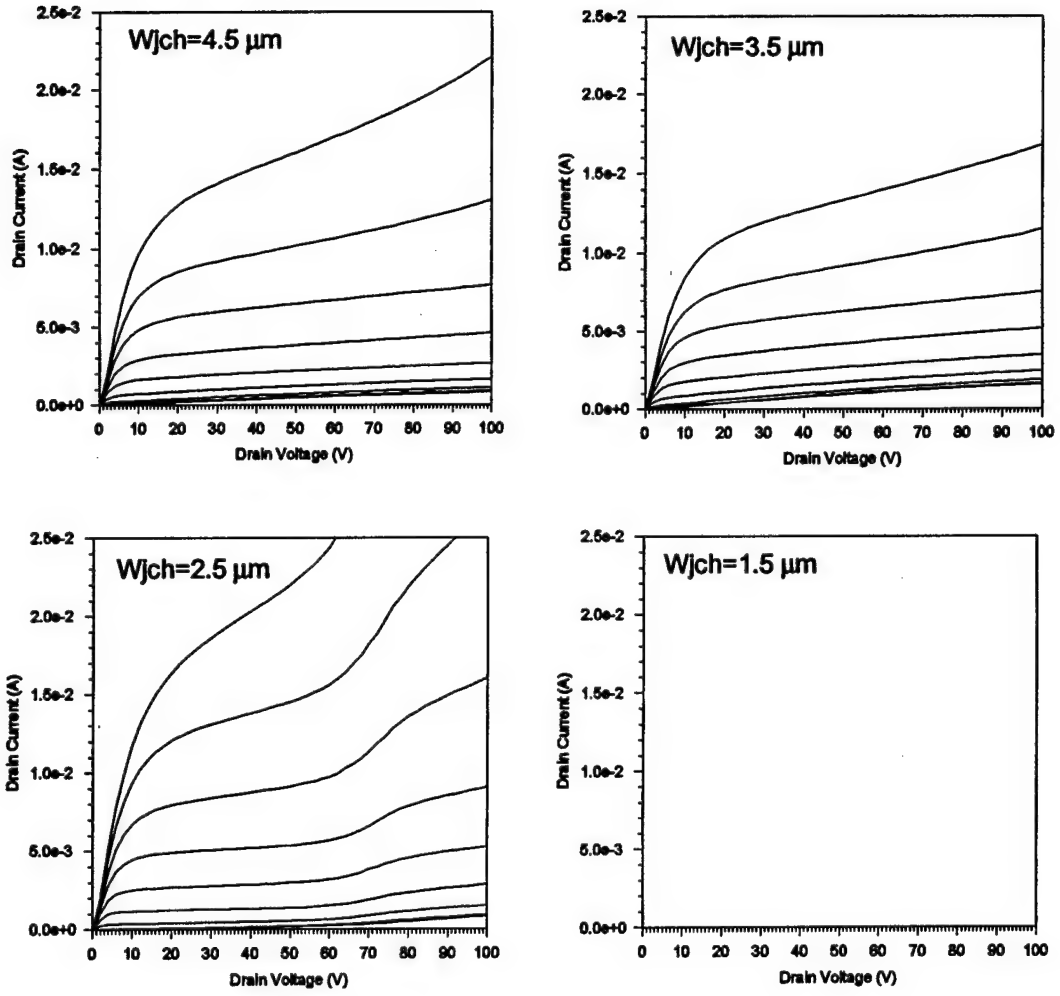

Fig. 1.15 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 3 on a 10 µm thick epilayer with a doping of $1x10^{16}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

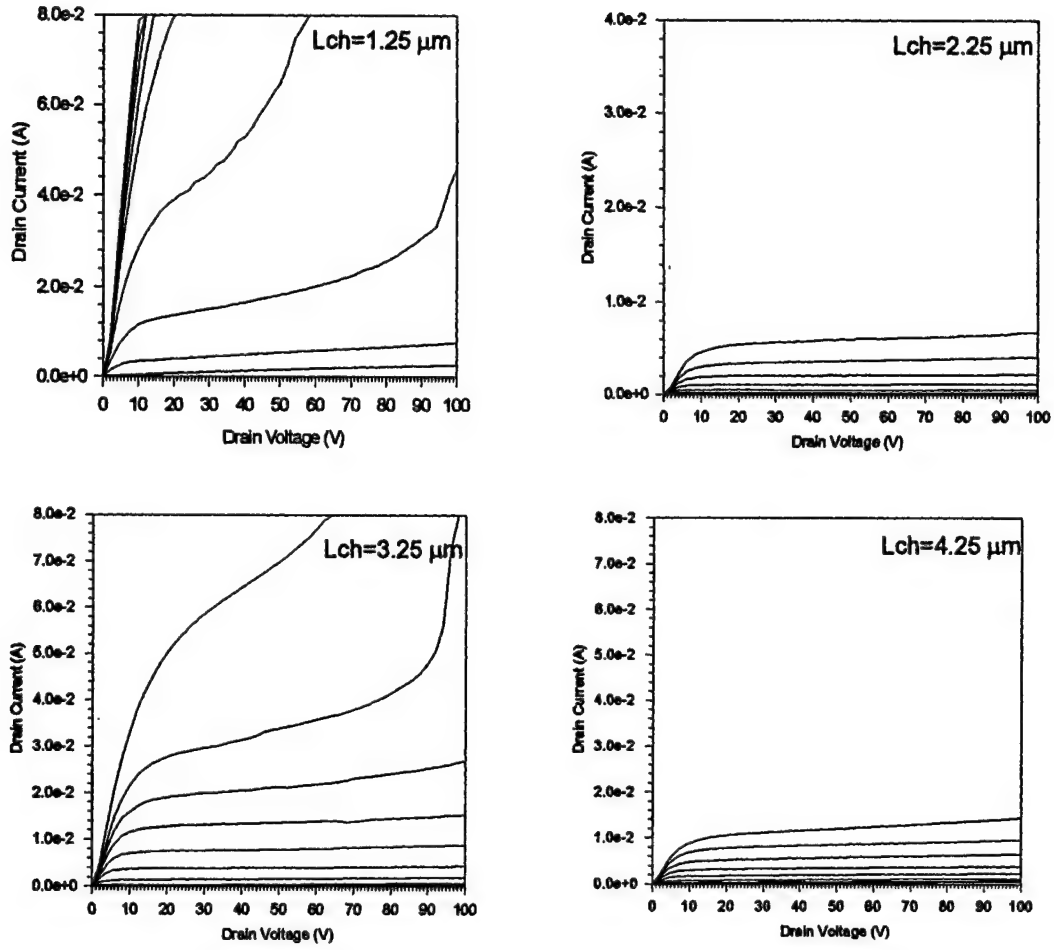

Fig. 1.16 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 1 on a 10 µm thick epilayer with a doping of $1x10^{16}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

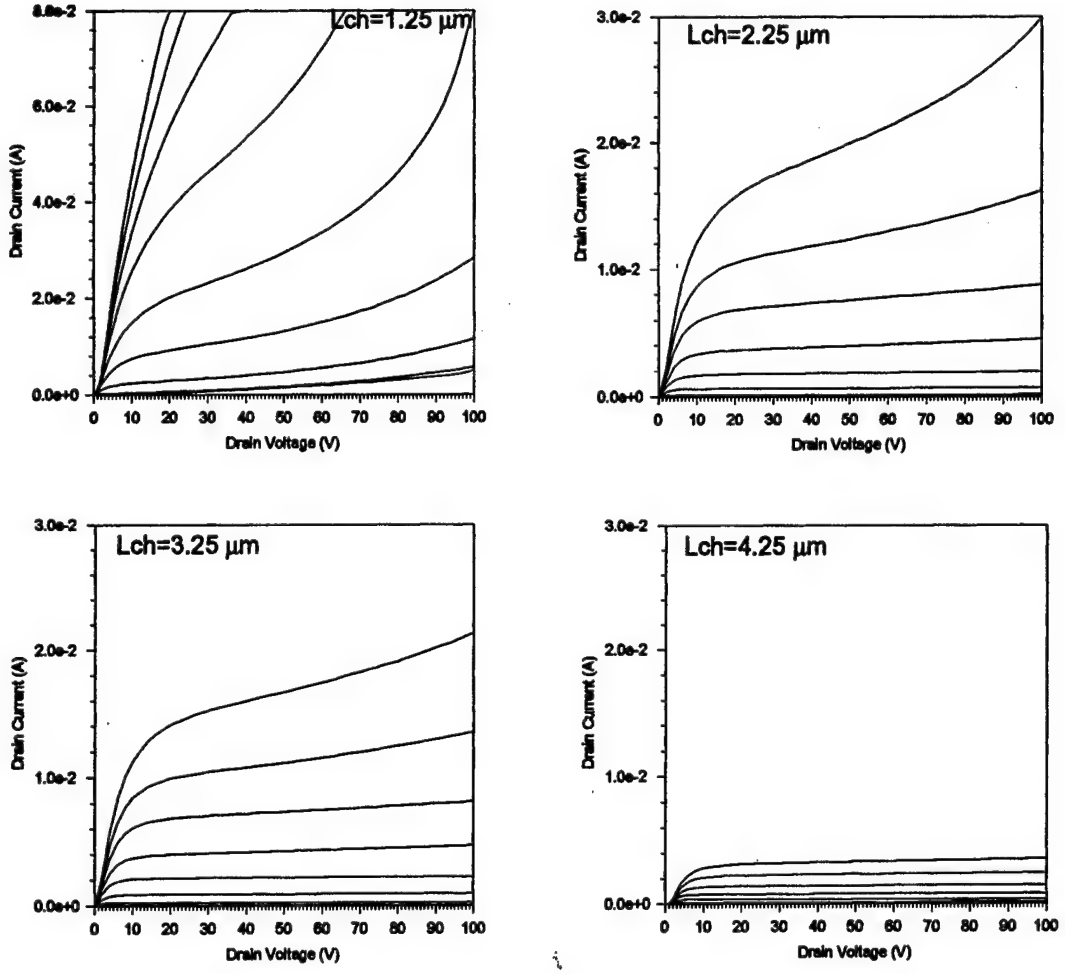

Fig. 1.17 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 2 on a 10 µm thick epilayer with a doping of $1x10^{16}$ cm^{-3}, at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

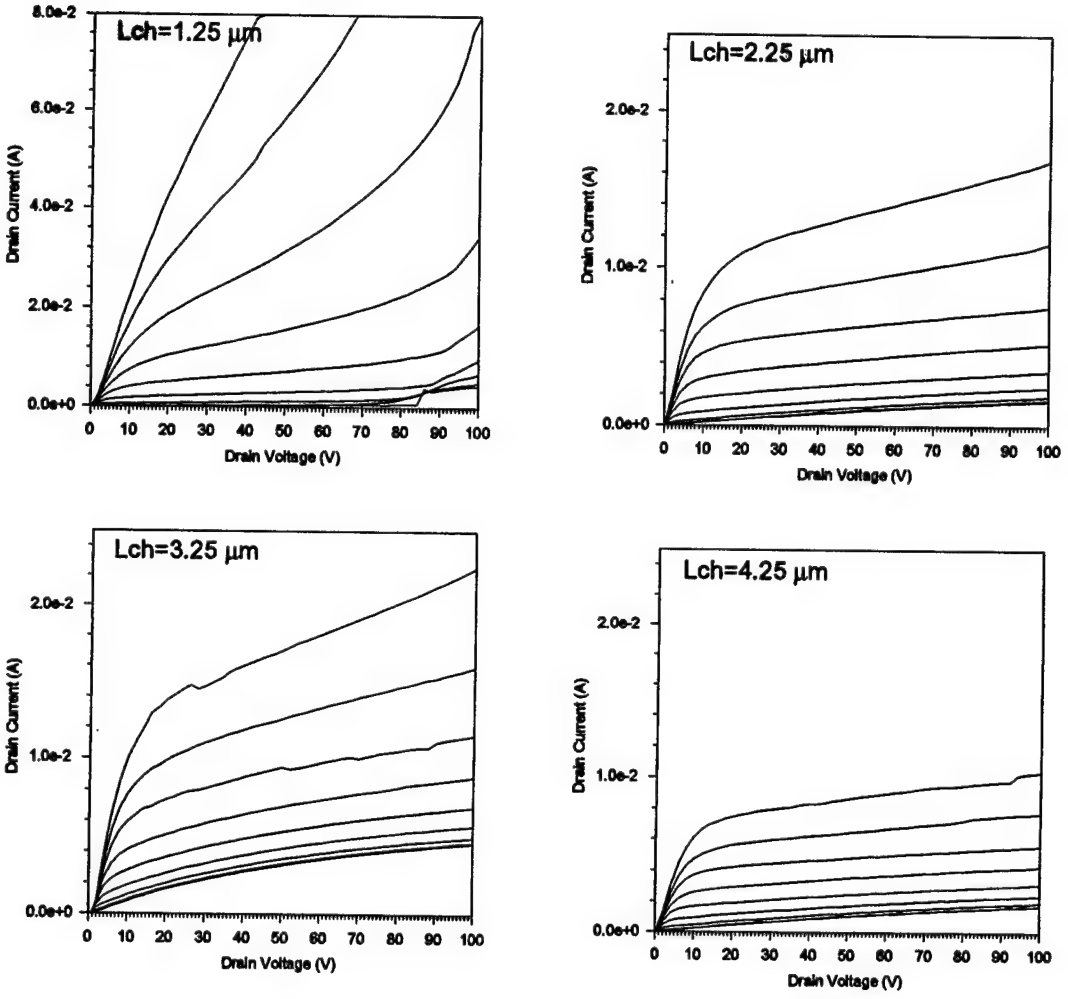

Fig. 1.18 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 3 on a 10 µm thick epilayer with a doping of $1x10^{16}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

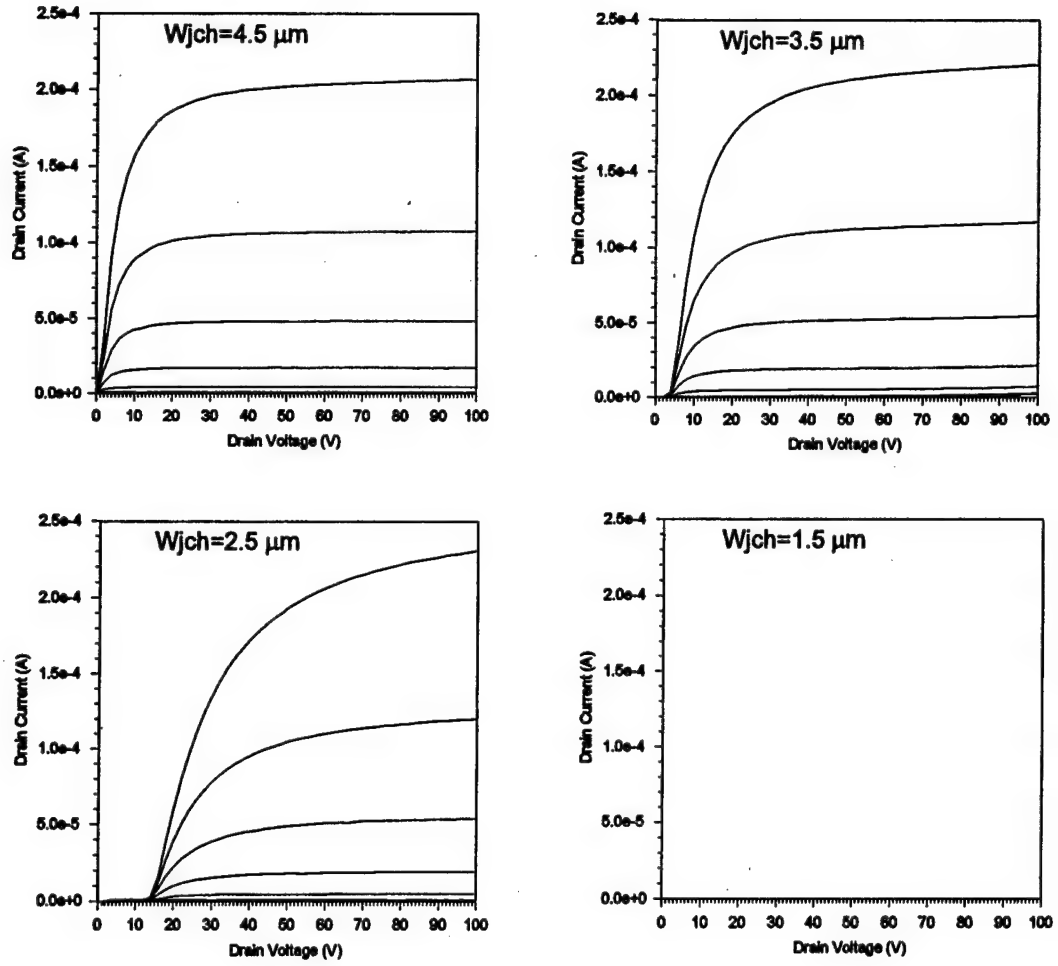

Fig. 1.19 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 1 on a 20 µm thick epilayer with a doping of $1.5x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

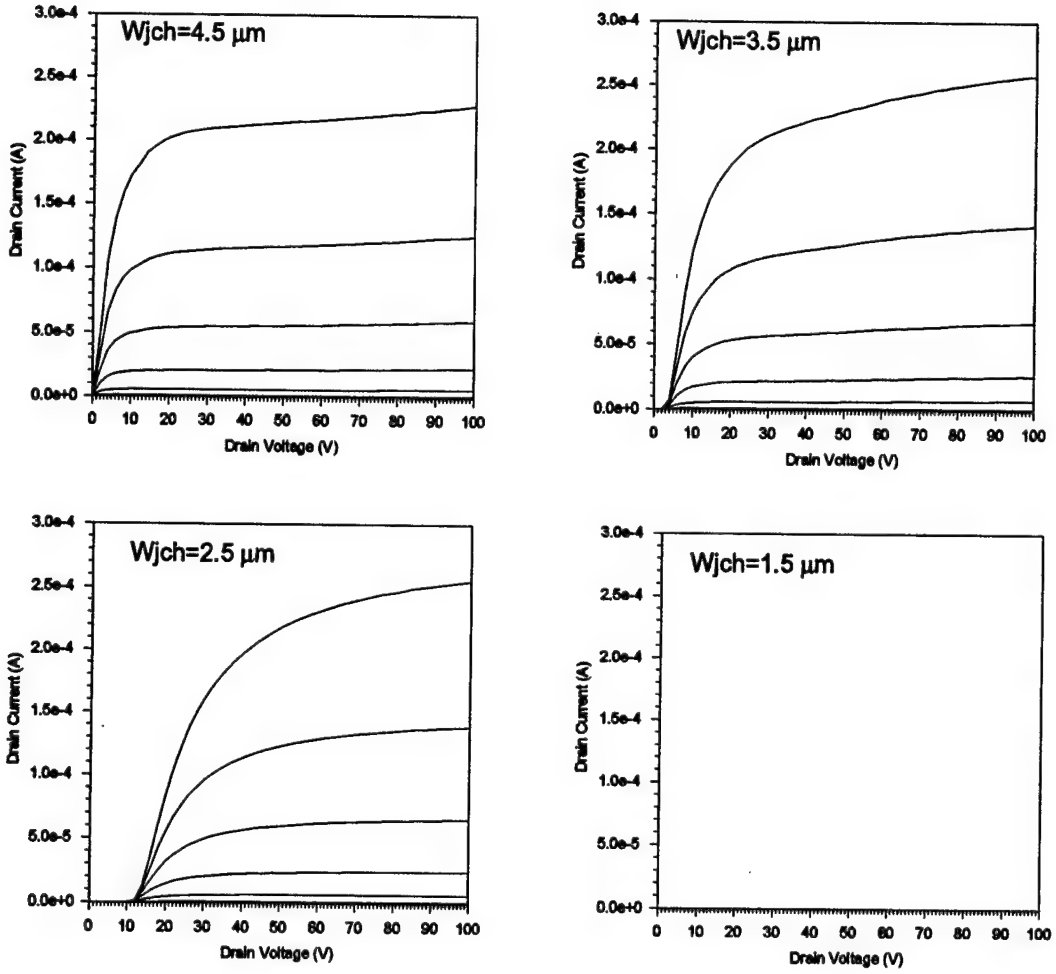

Fig. 1.20 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 2 on a 20 µm thick epilayer with a doping of $1.5x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

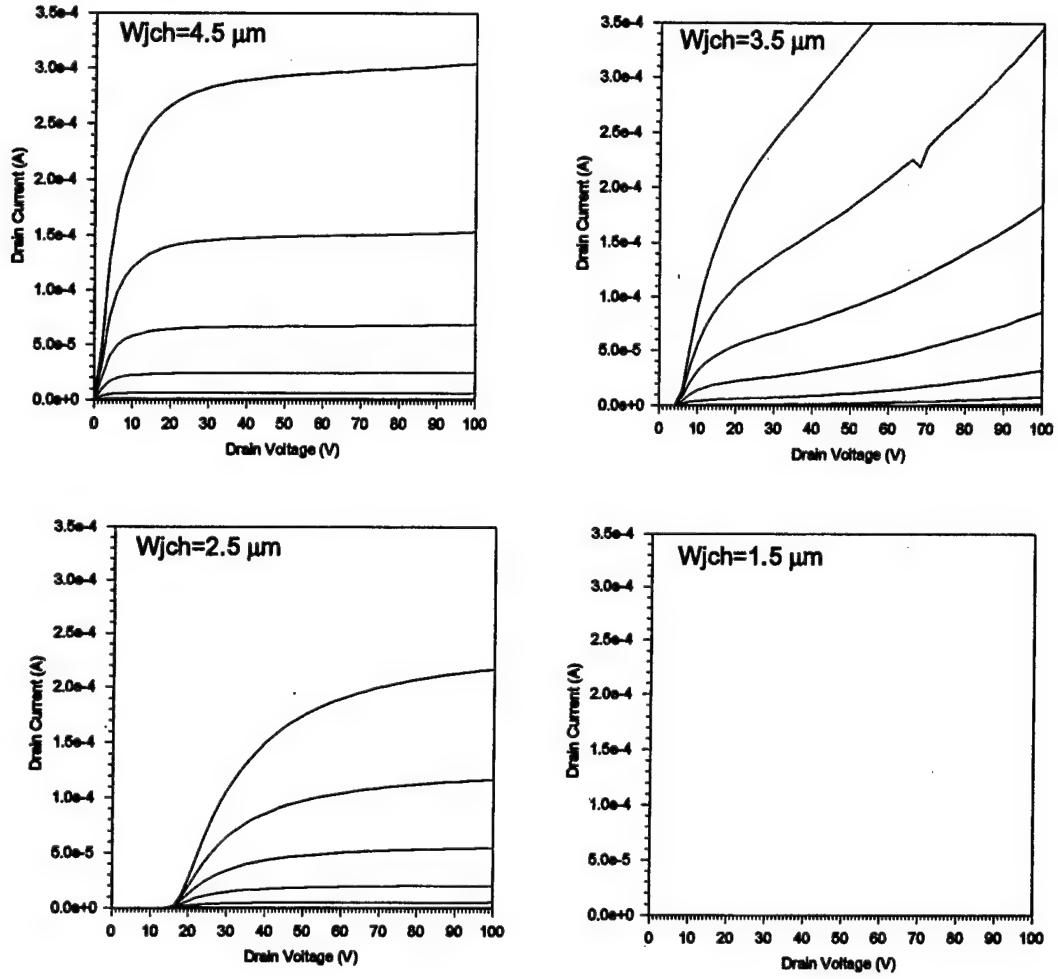

Fig. 1.21 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 3 on a 20 µm thick epilayer with a doping of $1.5x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

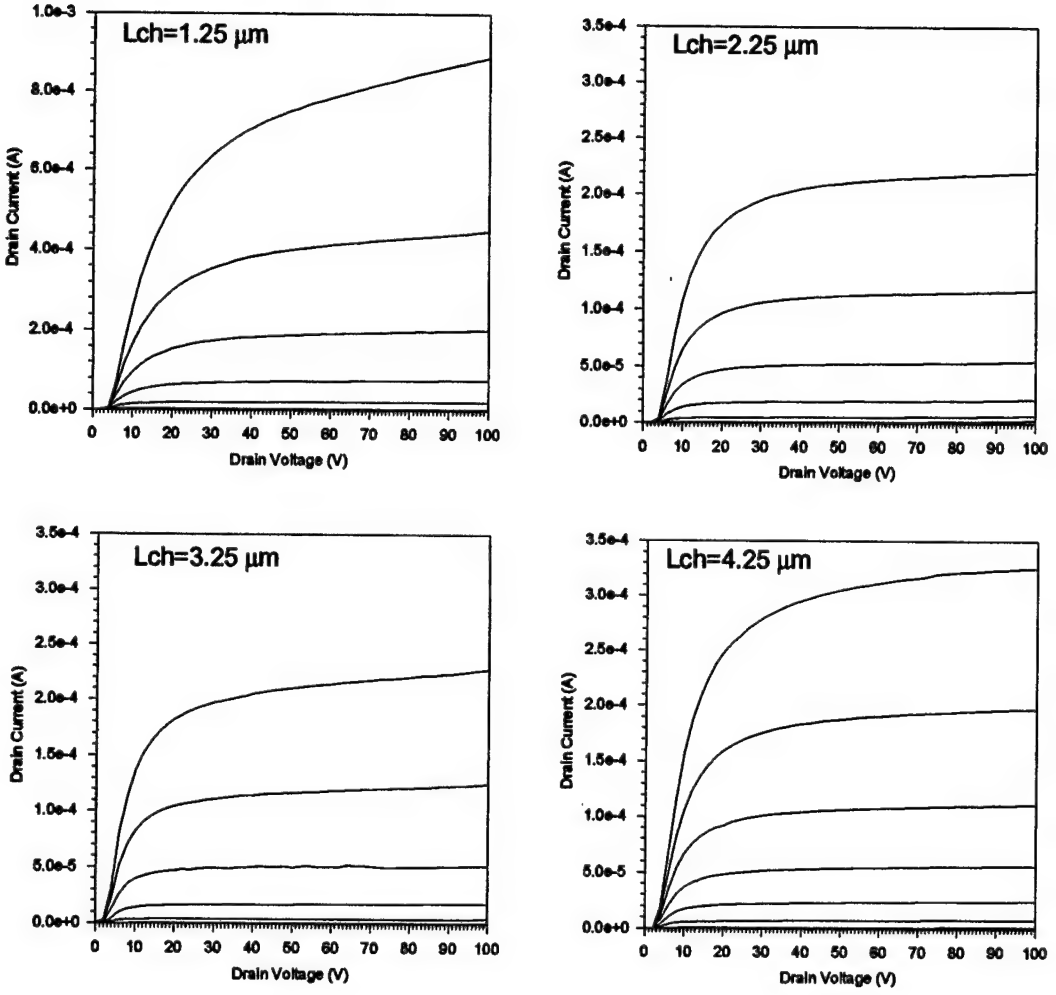

Fig. 1.22 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 1 on a 20 µm thick epilayer with a doping of $1.5x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

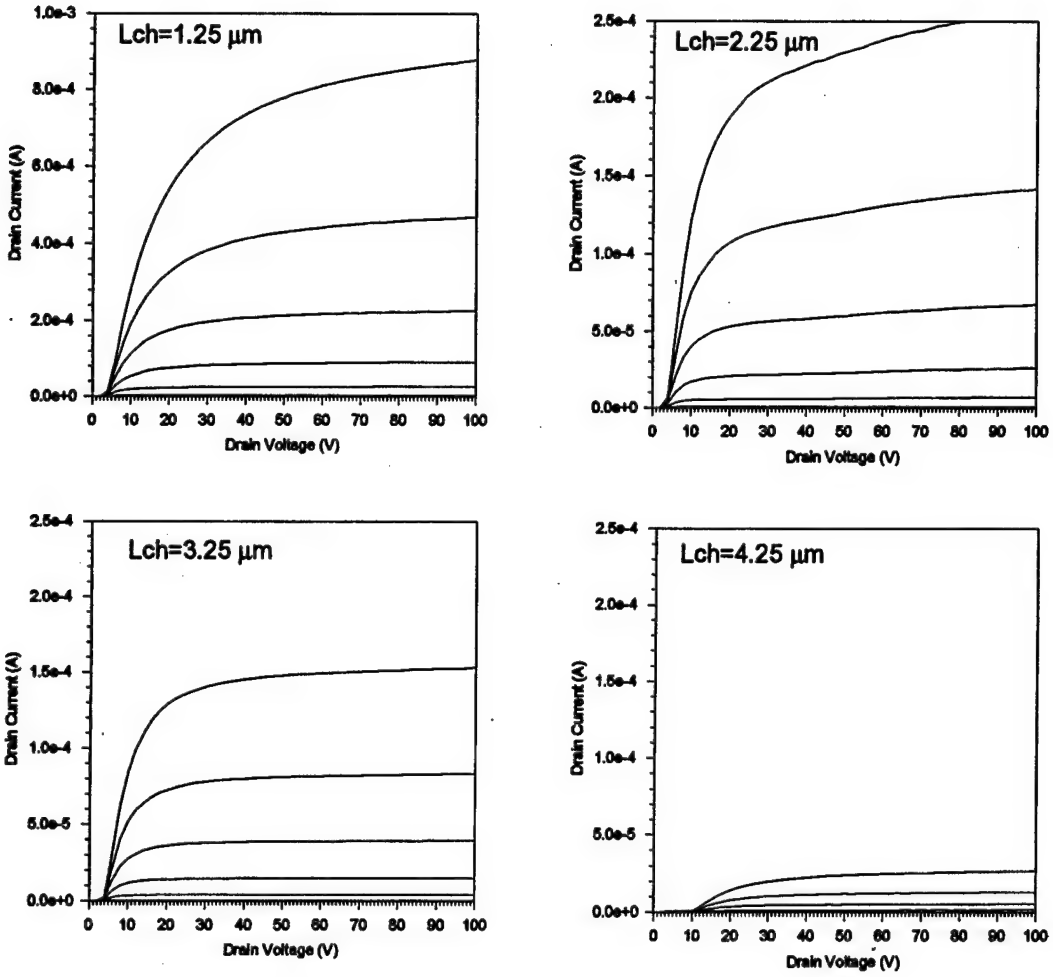

Fig. 1.23 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 2 on a 20 µm thick epilayer with a doping of 1.5×10^{15} cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

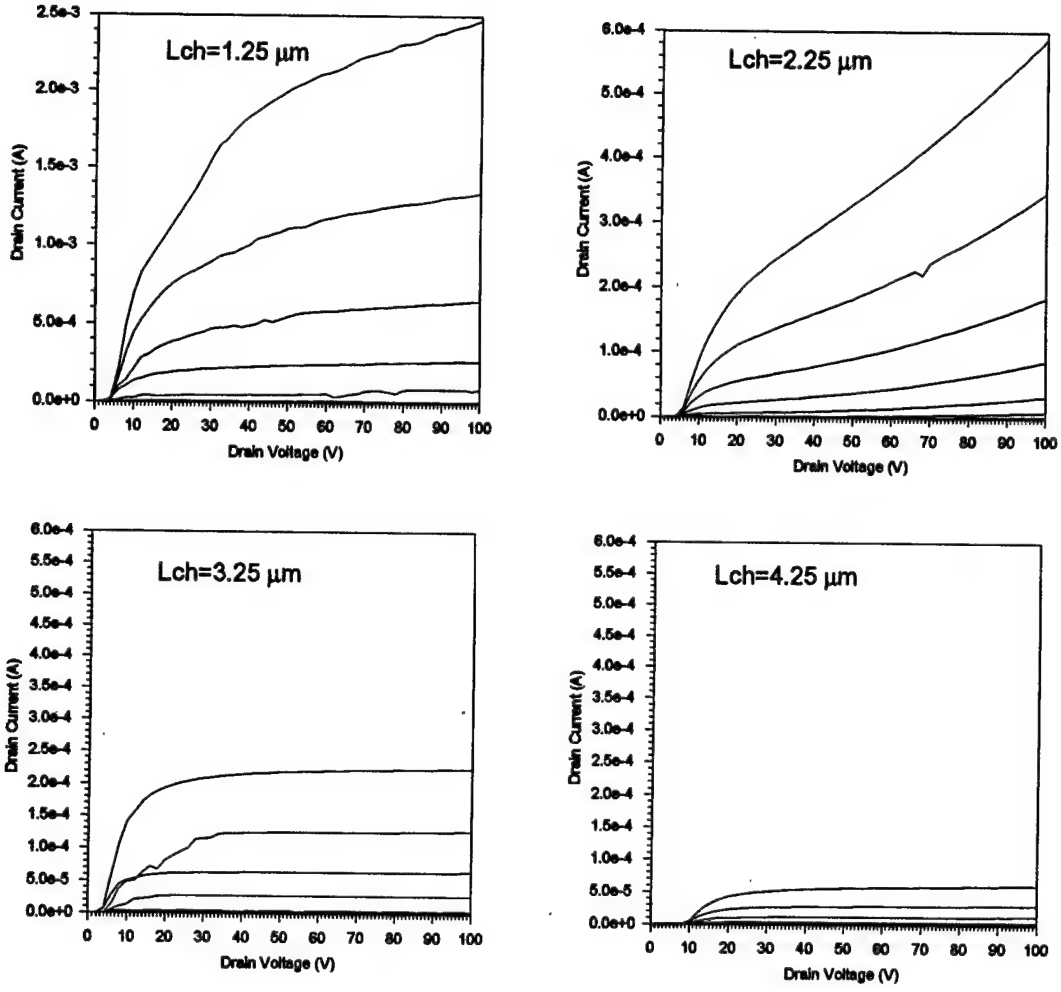

Fig. 1.24 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 3 on a 20 µm thick epilayer with a doping of 1.5×10^{15} cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

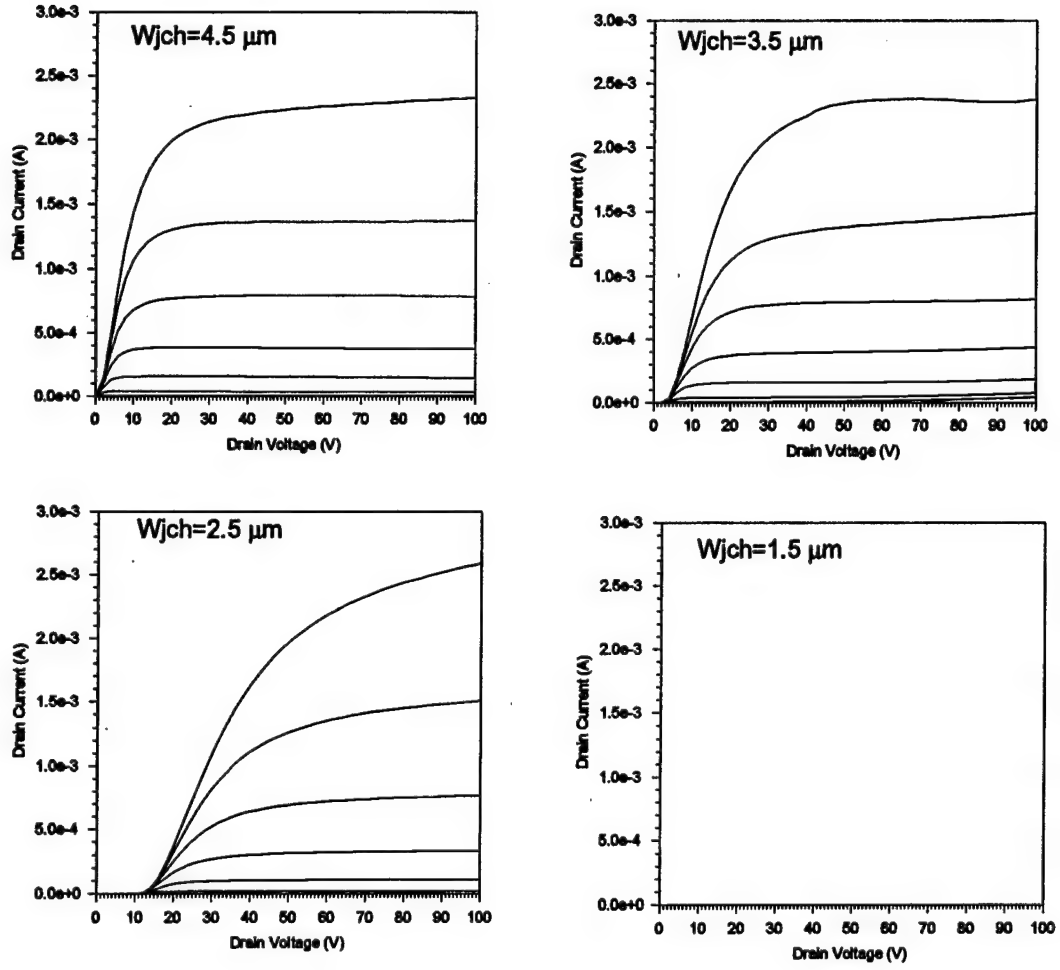

Fig. 1.25 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 1 on a 20 µm thick epilayer with a doping of $1.5x10^{15}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

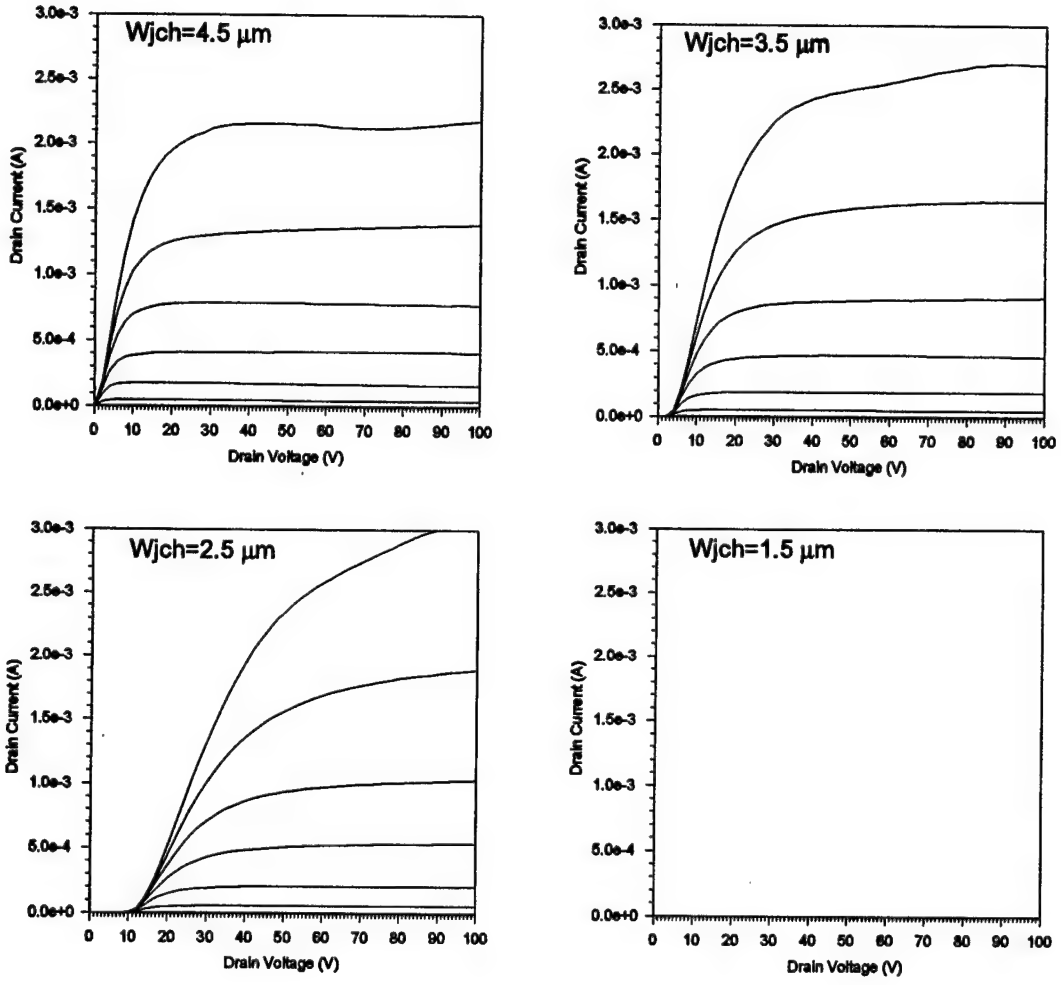

Fig. 1.26 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 2 on a 20 µm thick epilayer with a doping of $1.5x10^{15}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

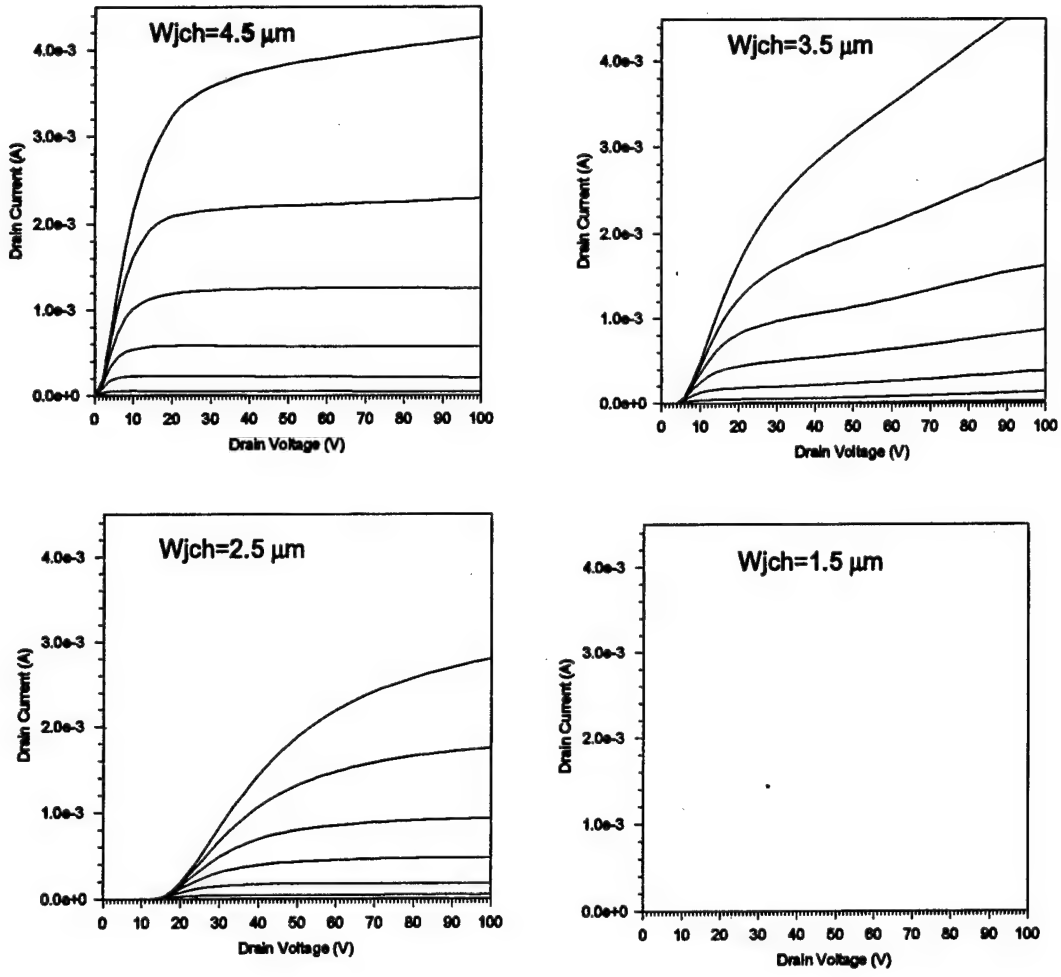

Fig. 1.27 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 3 on a 20 µm thick epilayer with a doping of $1.5x10^{15}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

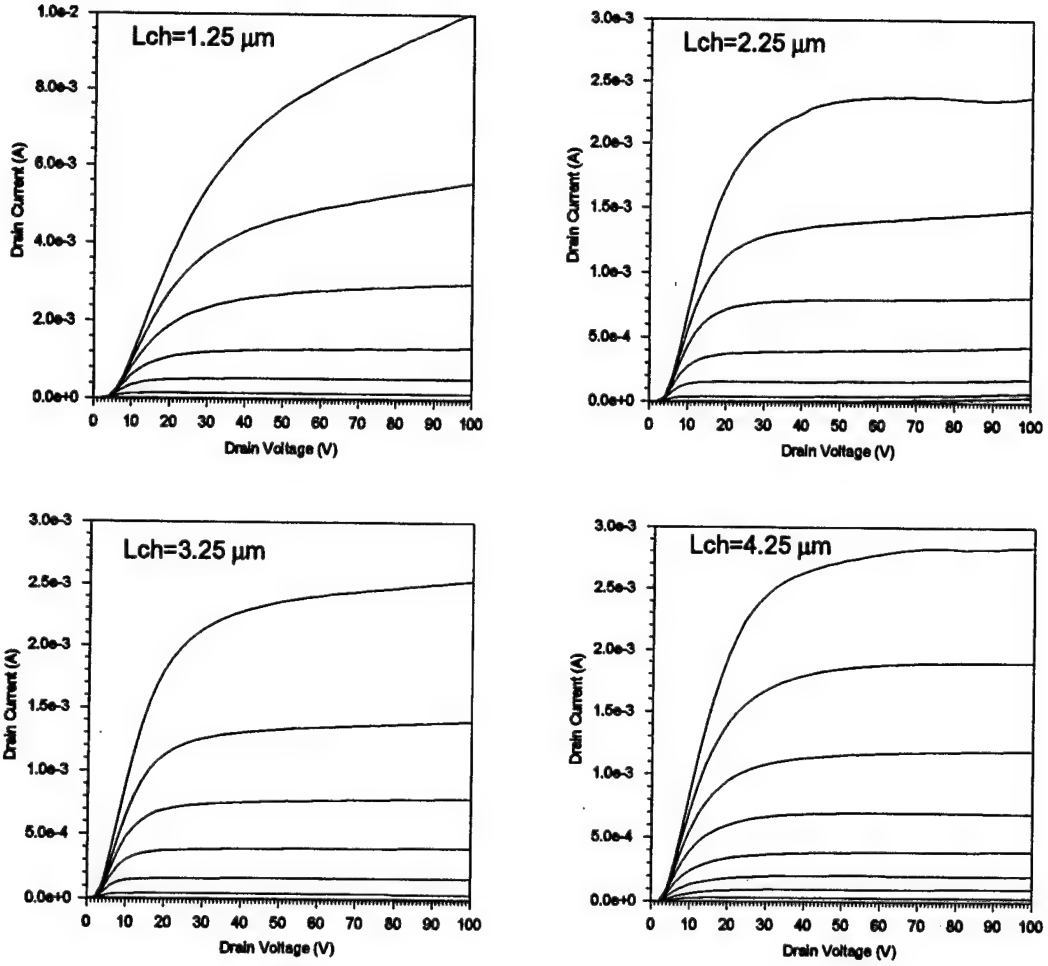

Fig. 1.28 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 1 on a 20 µm thick epilayer with a doping of $1.5x10^{15}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

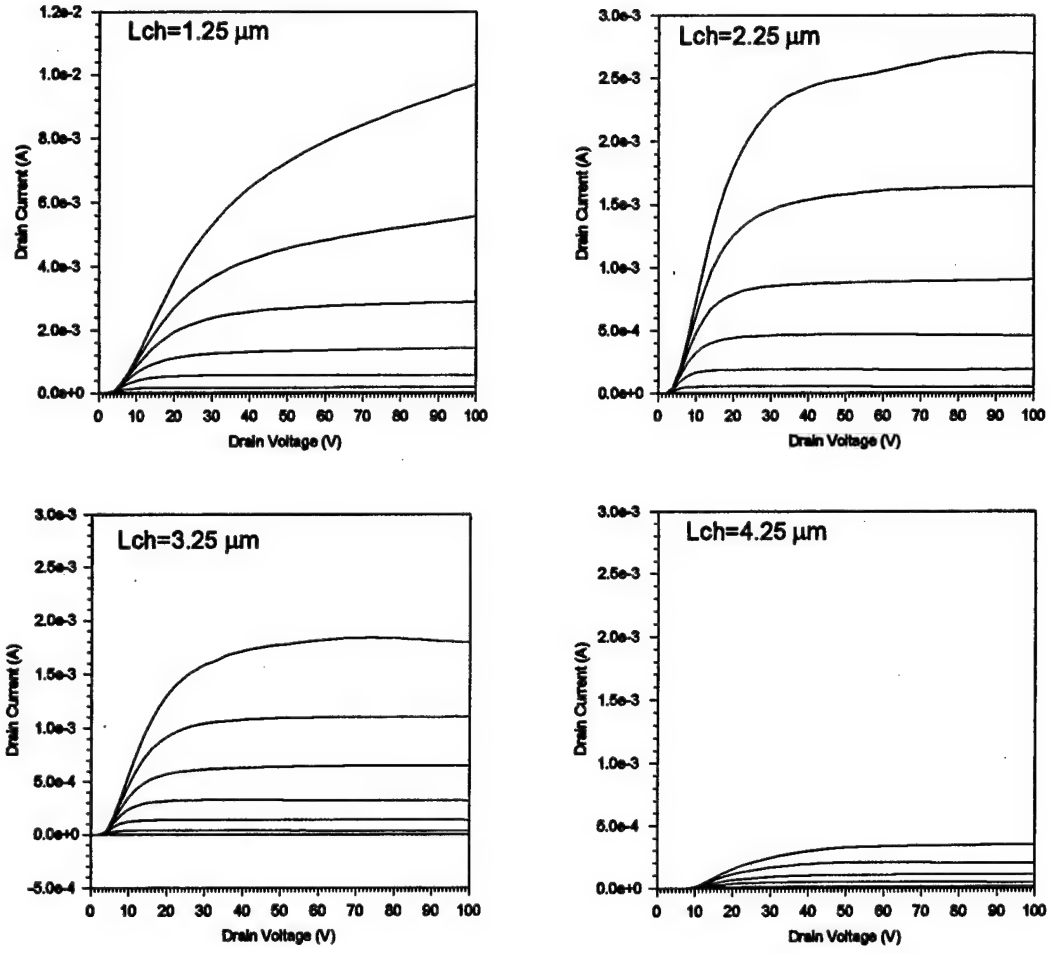

Fig. 1.29 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 2 on a 20 µm thick epilayer with a doping of 1.5×10^{15} cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

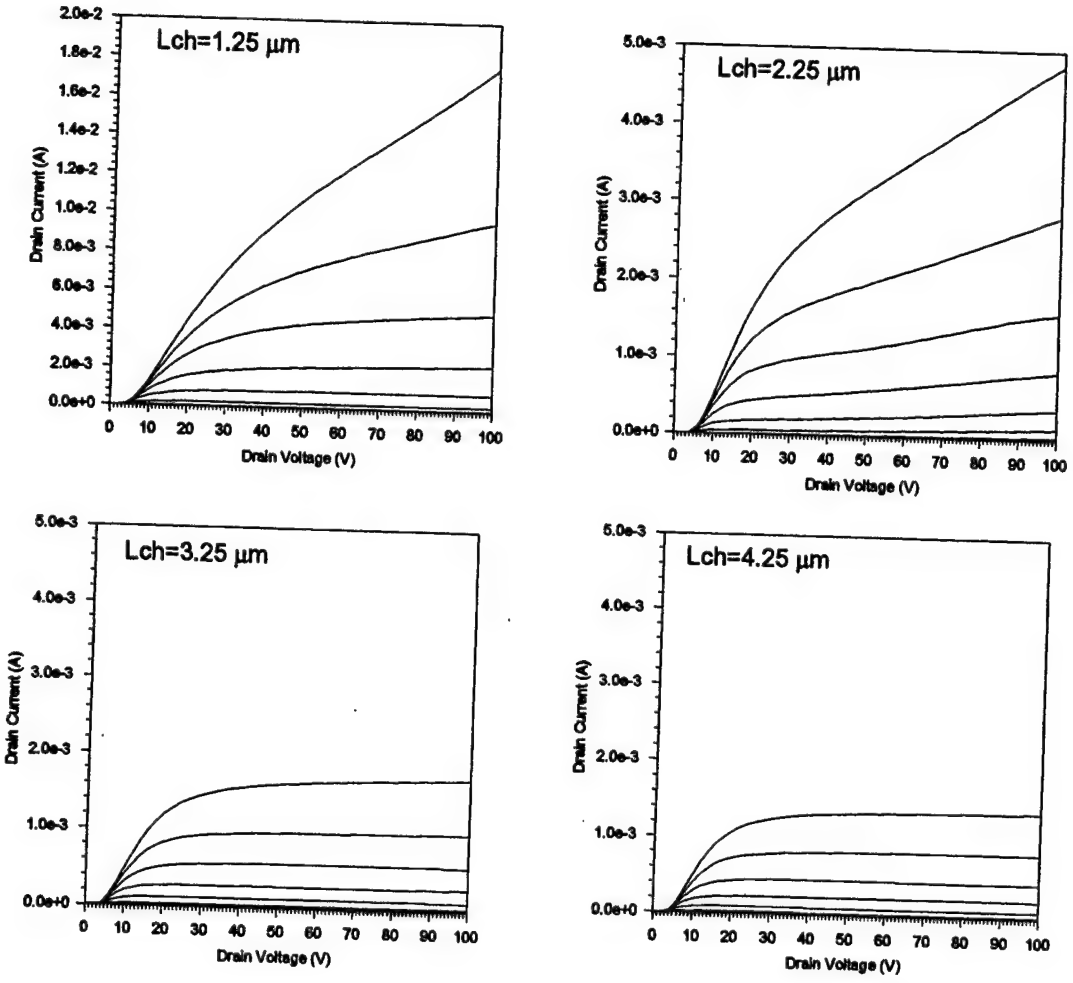

Fig. 1.30 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 3 on a 20 µm thick epilayer with a doping of 1.5×10^{15} cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

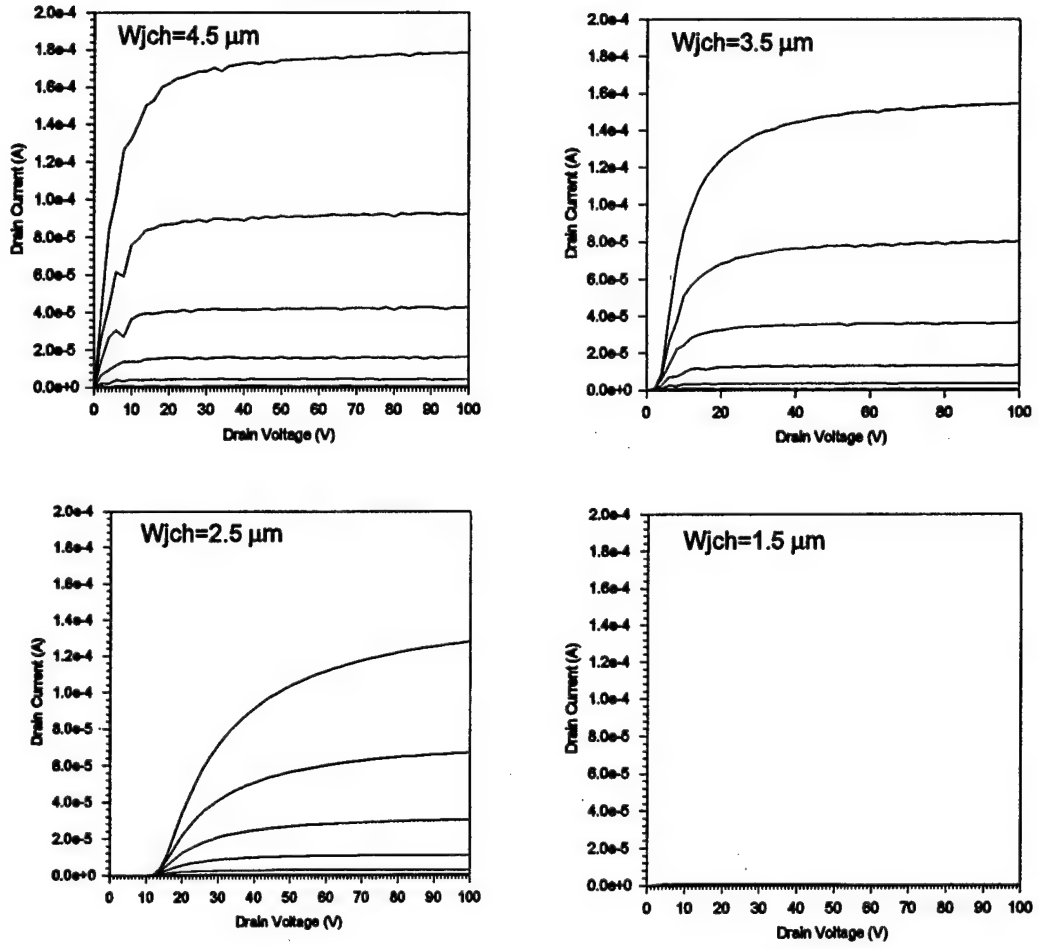

Fig. 1.31 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 1 on a 30 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

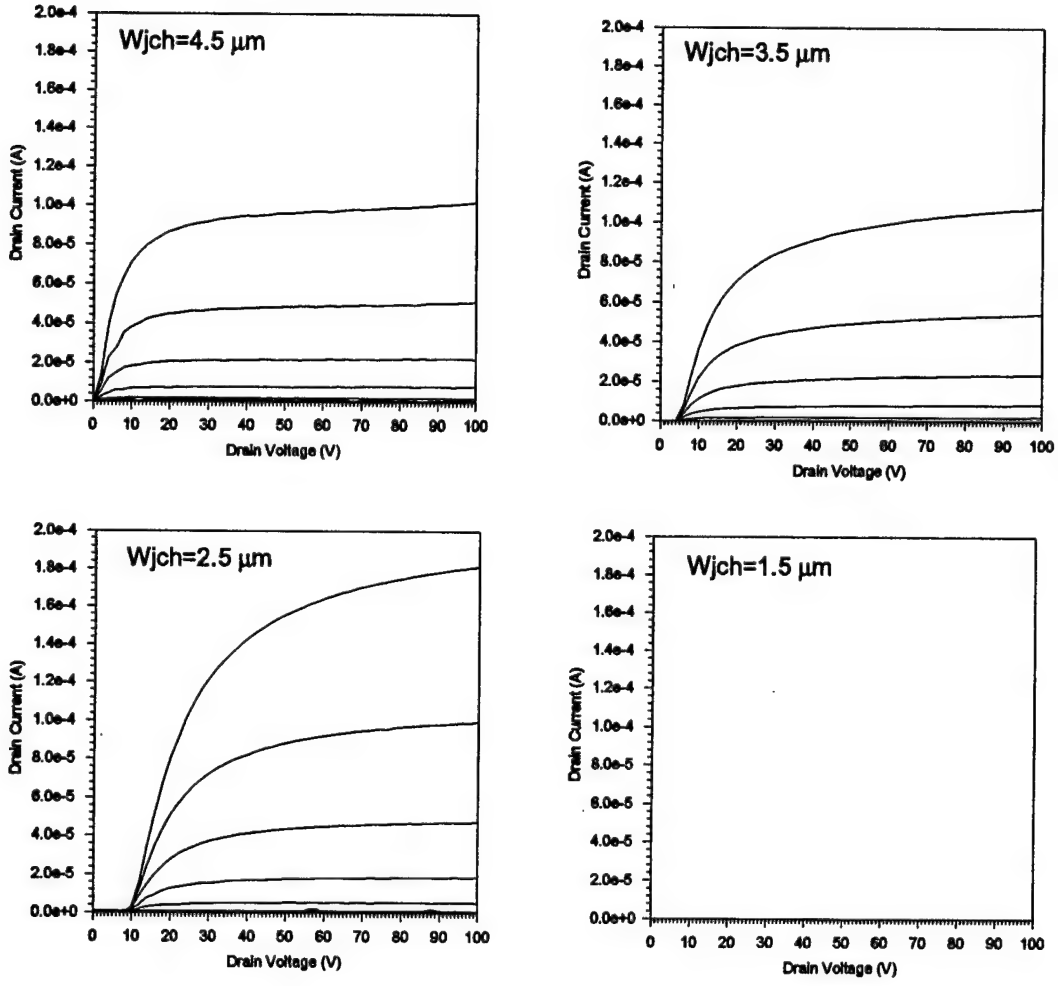

Fig. 1.32 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 2 on a 30 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

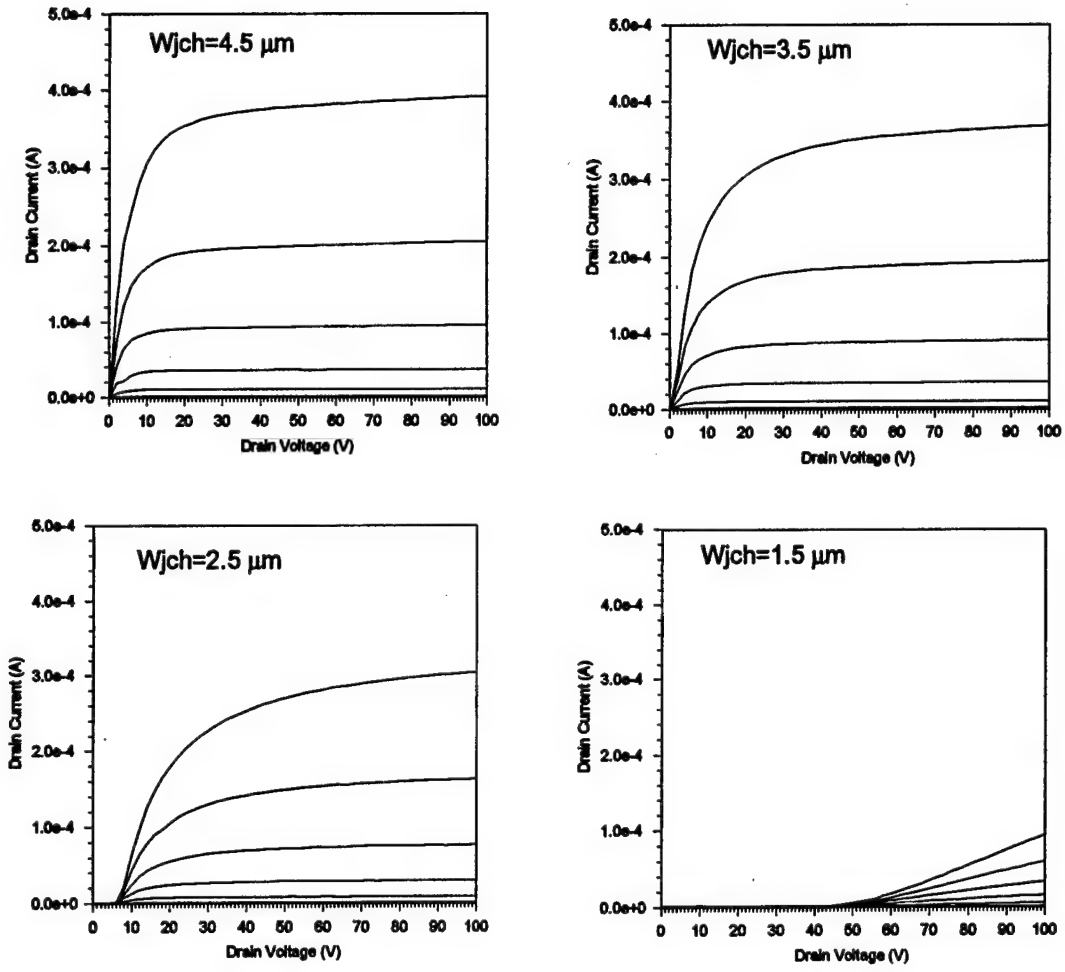

Fig. 1.33 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 3 on a 30 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

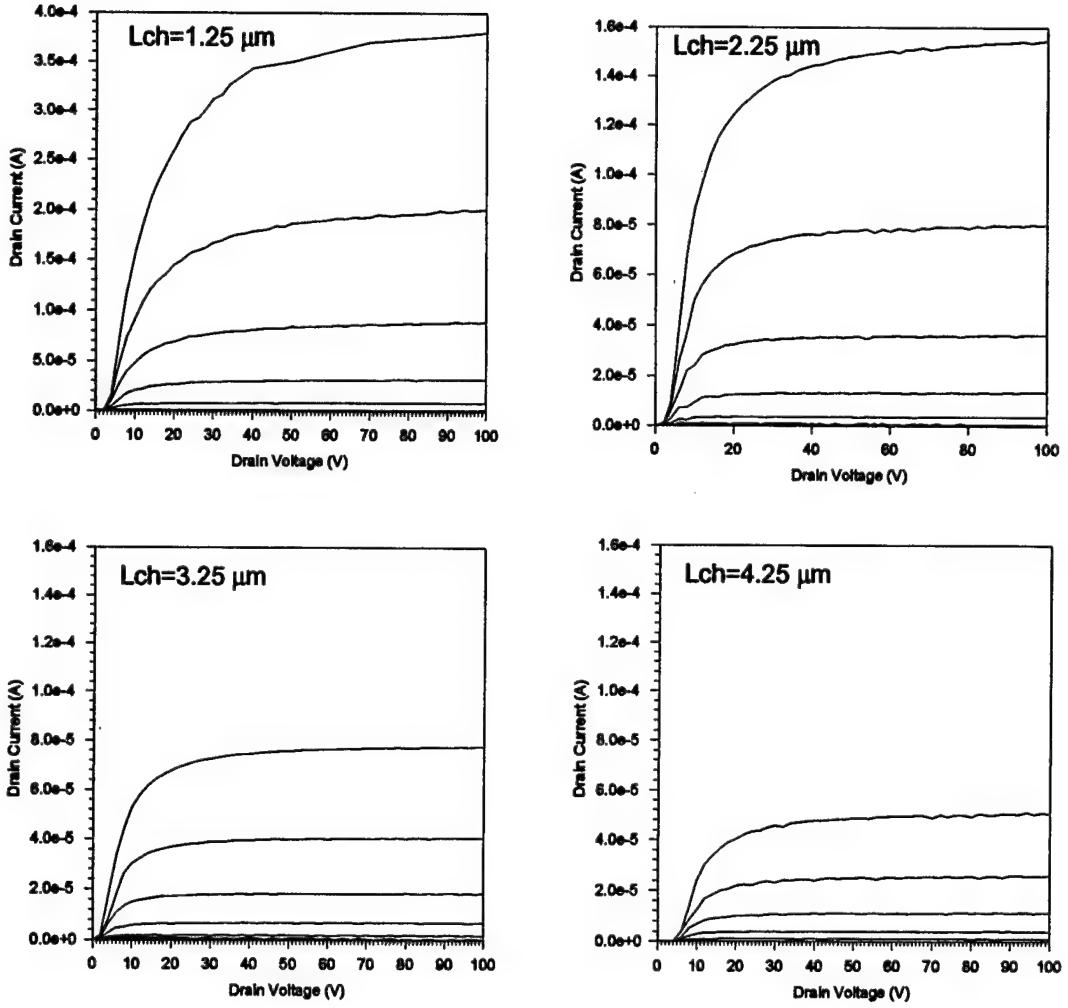

Fig. 1.34 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 1 on a 30 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

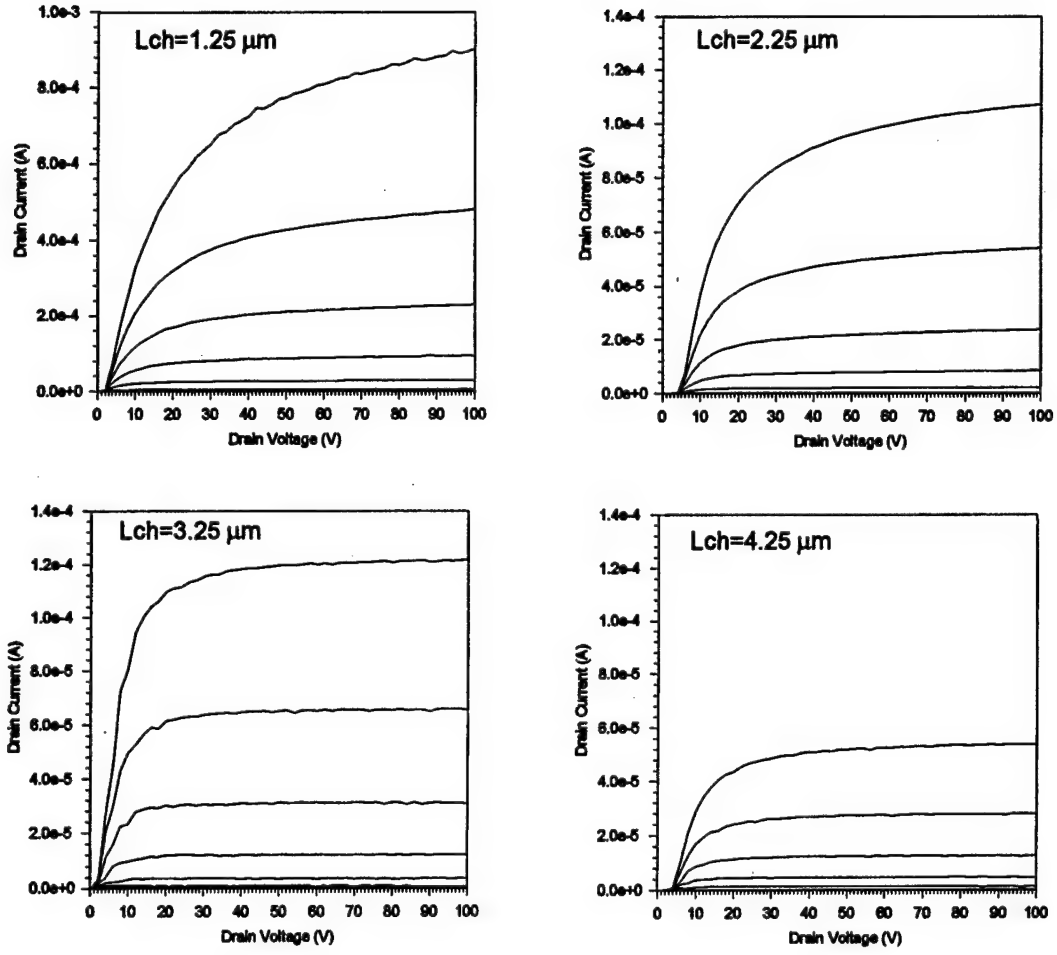

Fig. 1.35 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 2 on a 30 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

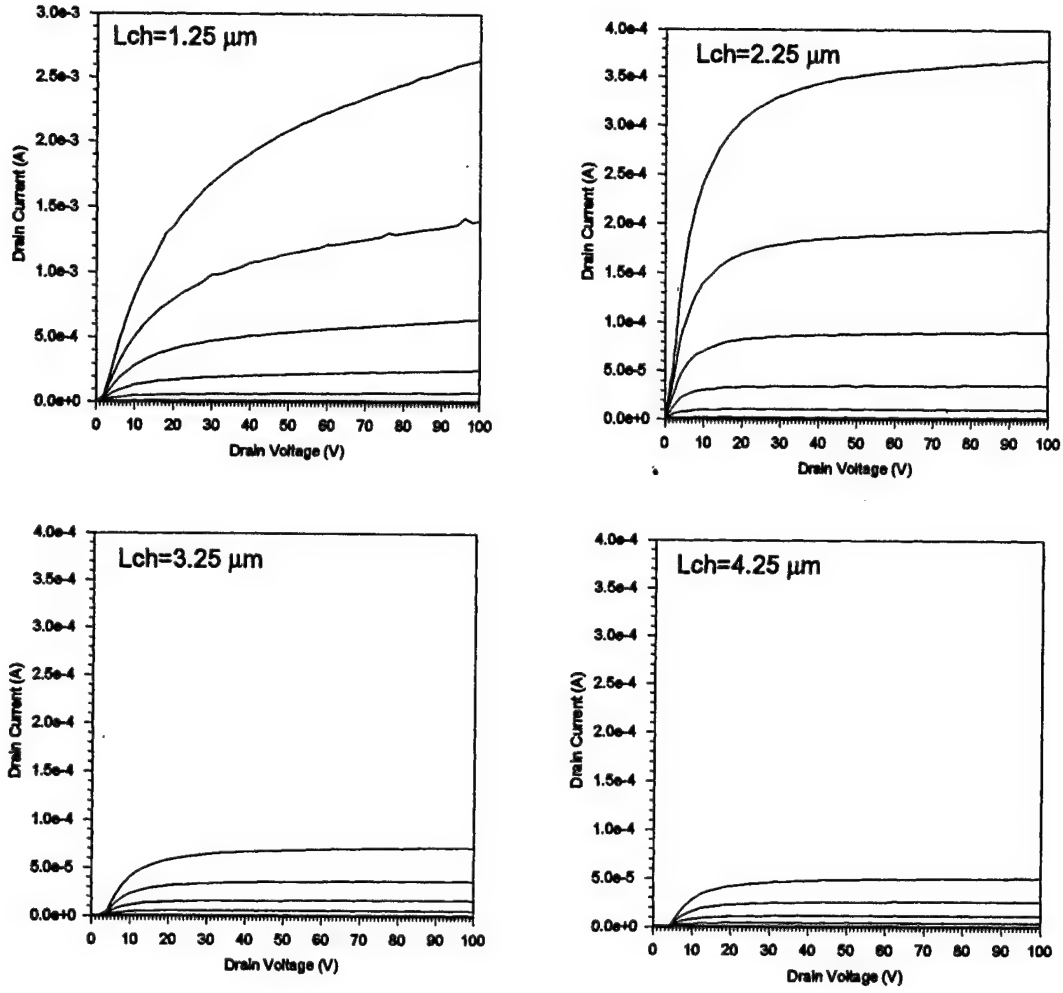

Fig. 1.36 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 3 on a 30 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

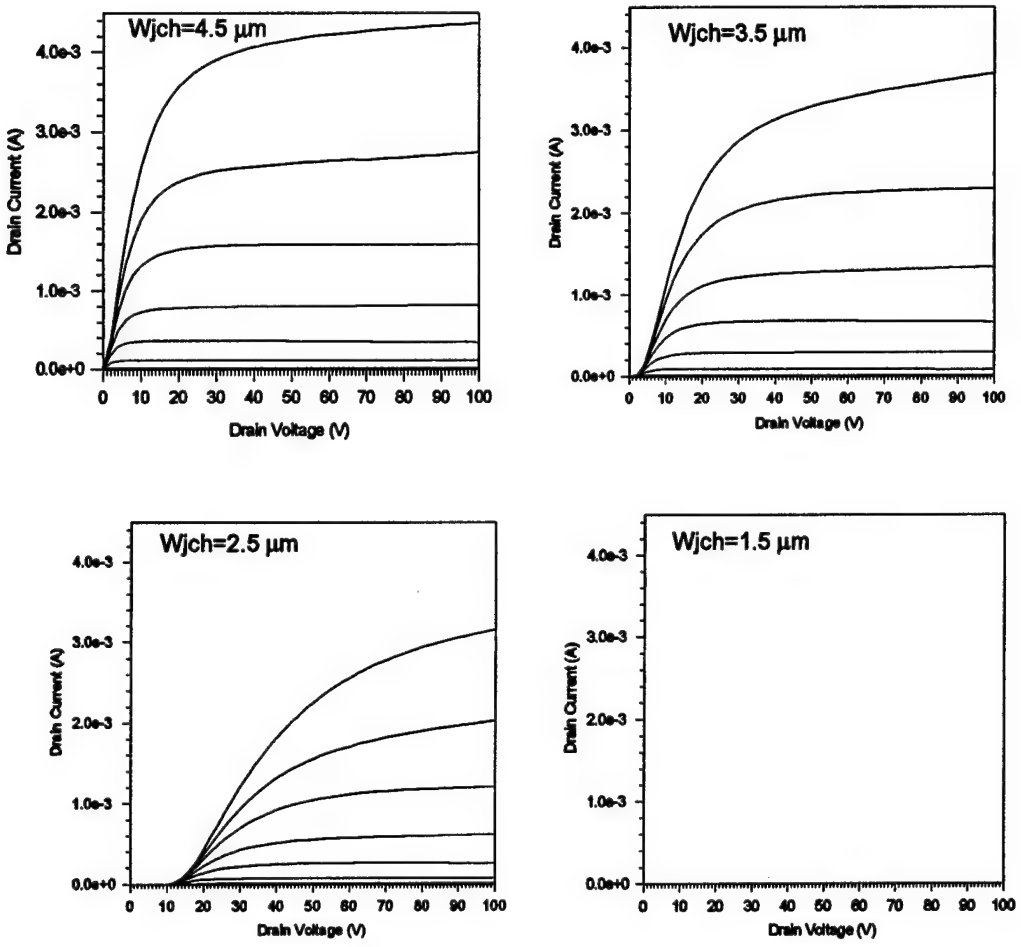

Fig. 1.37 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 1 on a 30 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

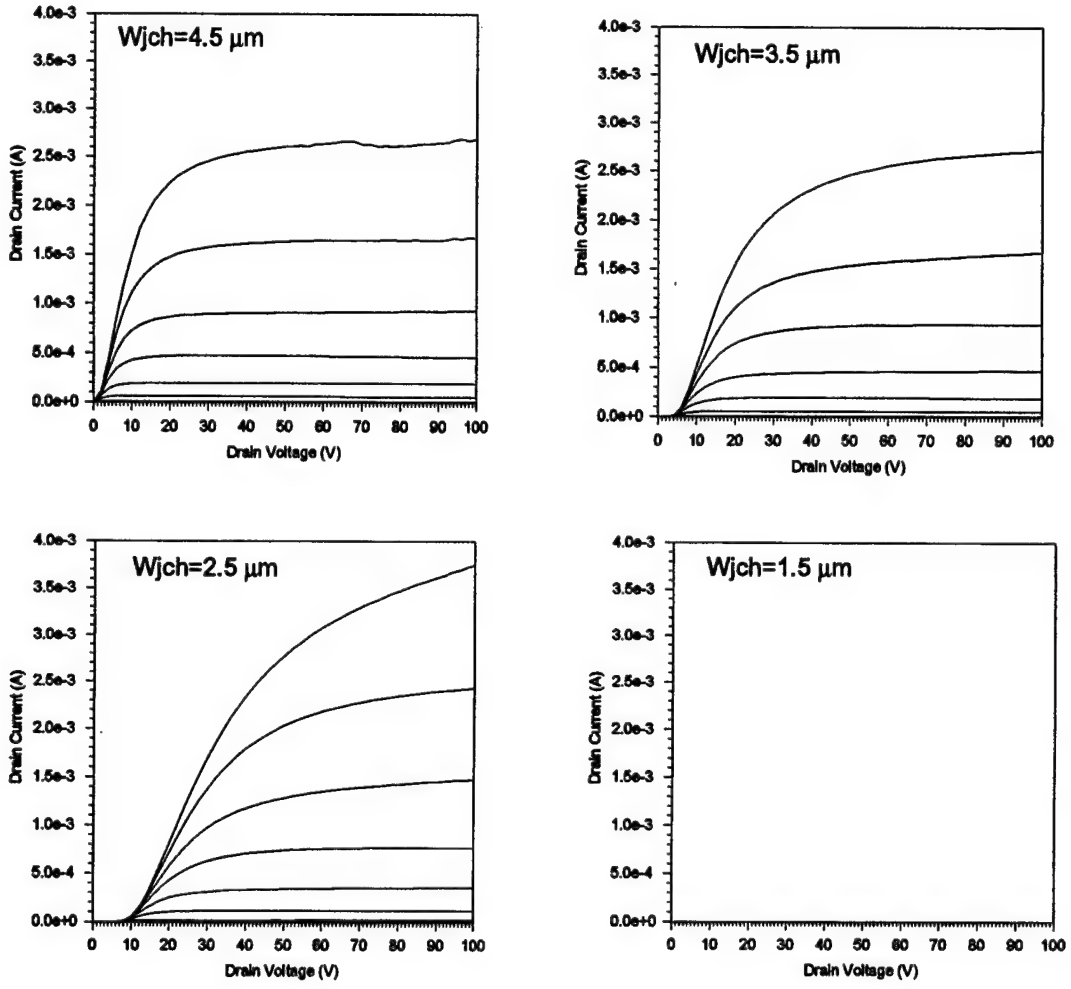

Fig. 1.38 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 2 on a 30 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

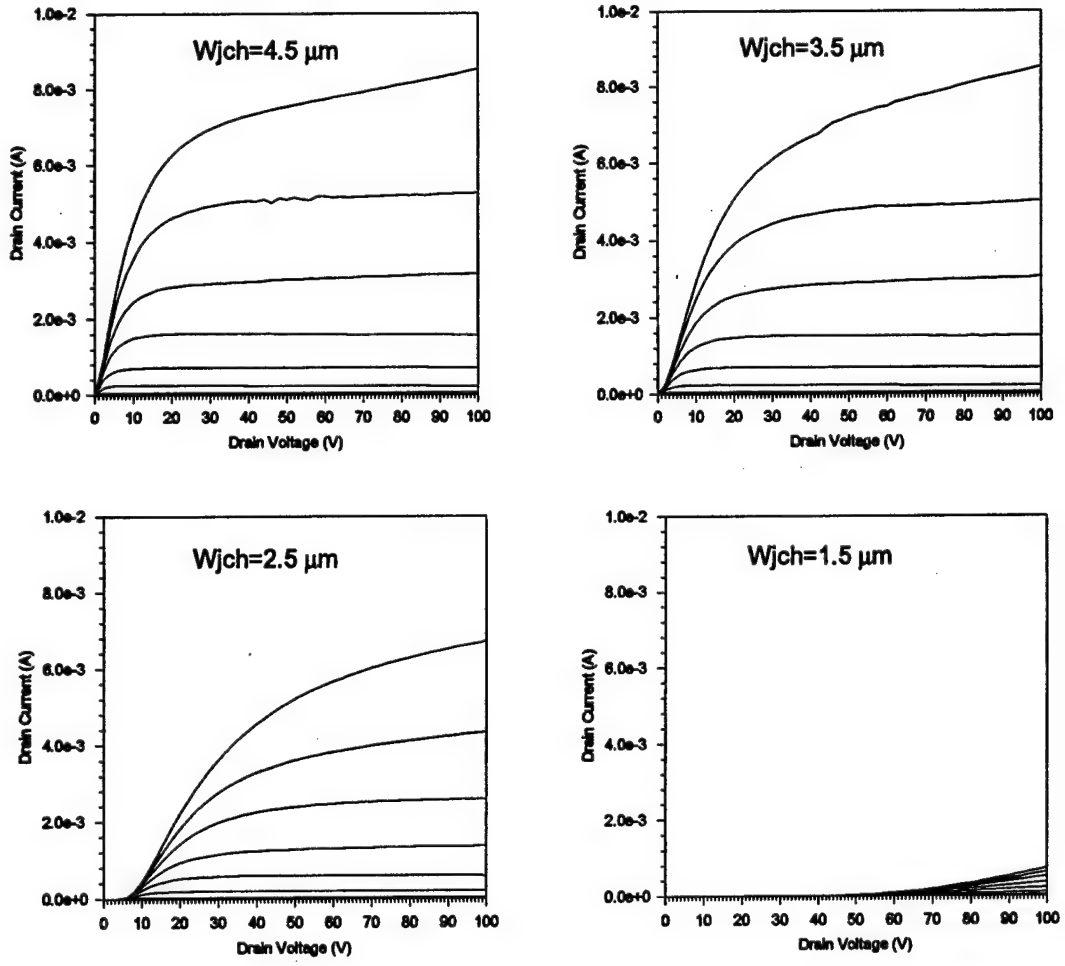

Fig. 1.39 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 3 on a 30 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

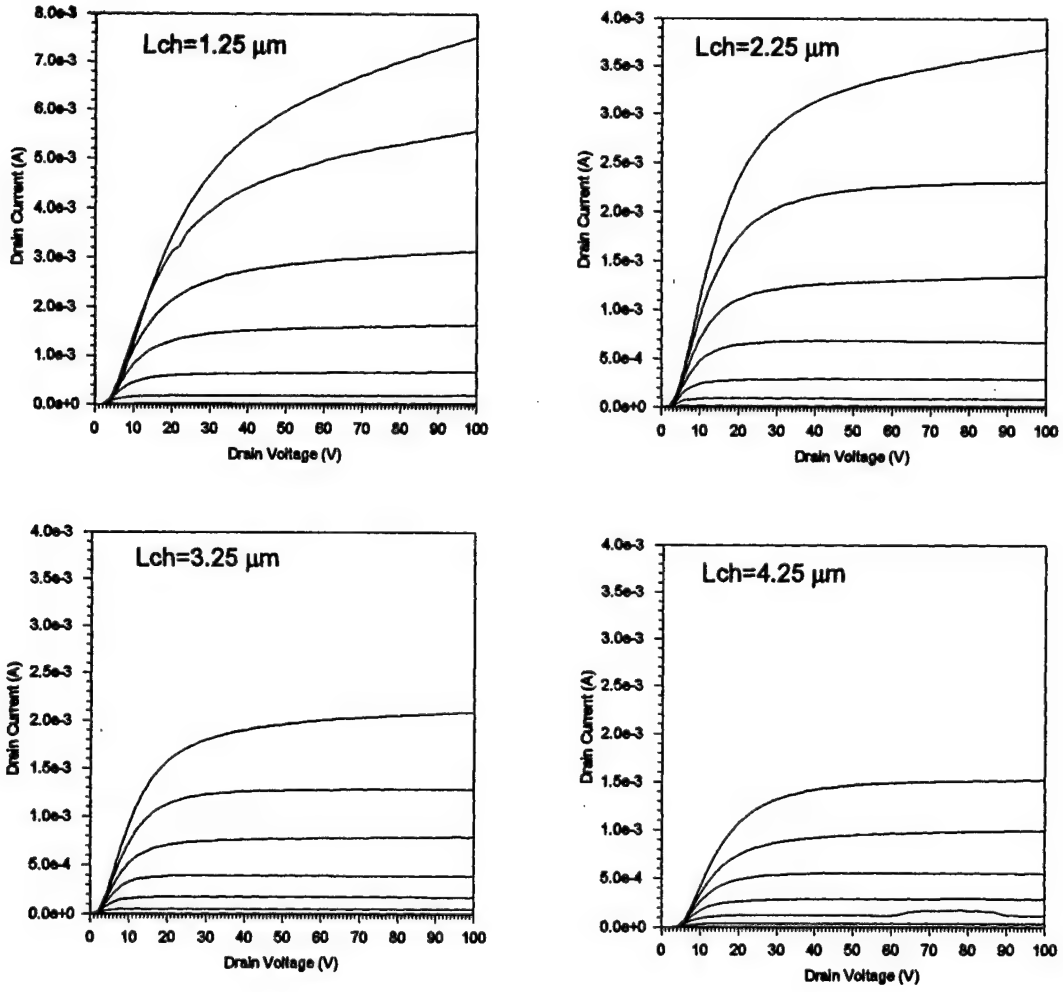

Fig. 1.40 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 1 on a 30 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

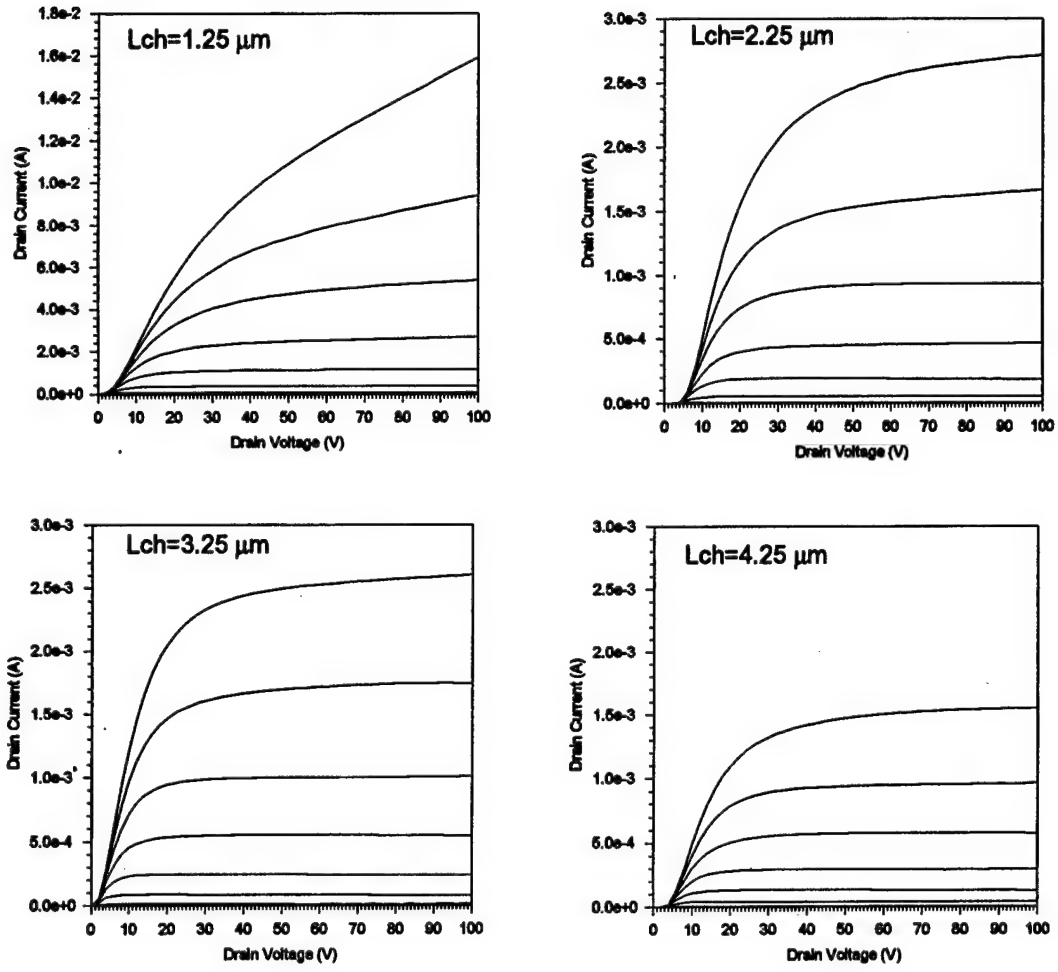

Fig. 1.41 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 2 on a 30 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

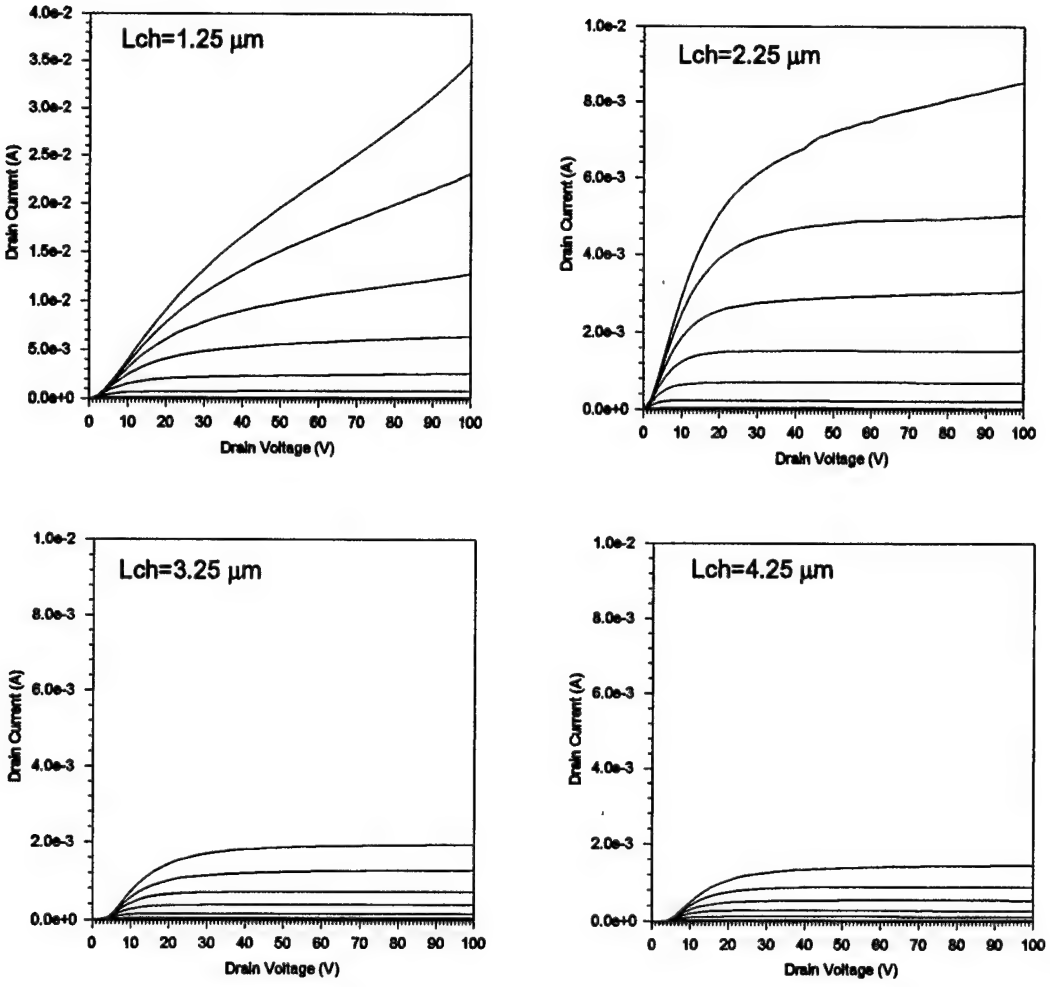

Fig. 1.42 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 3 on a 30 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

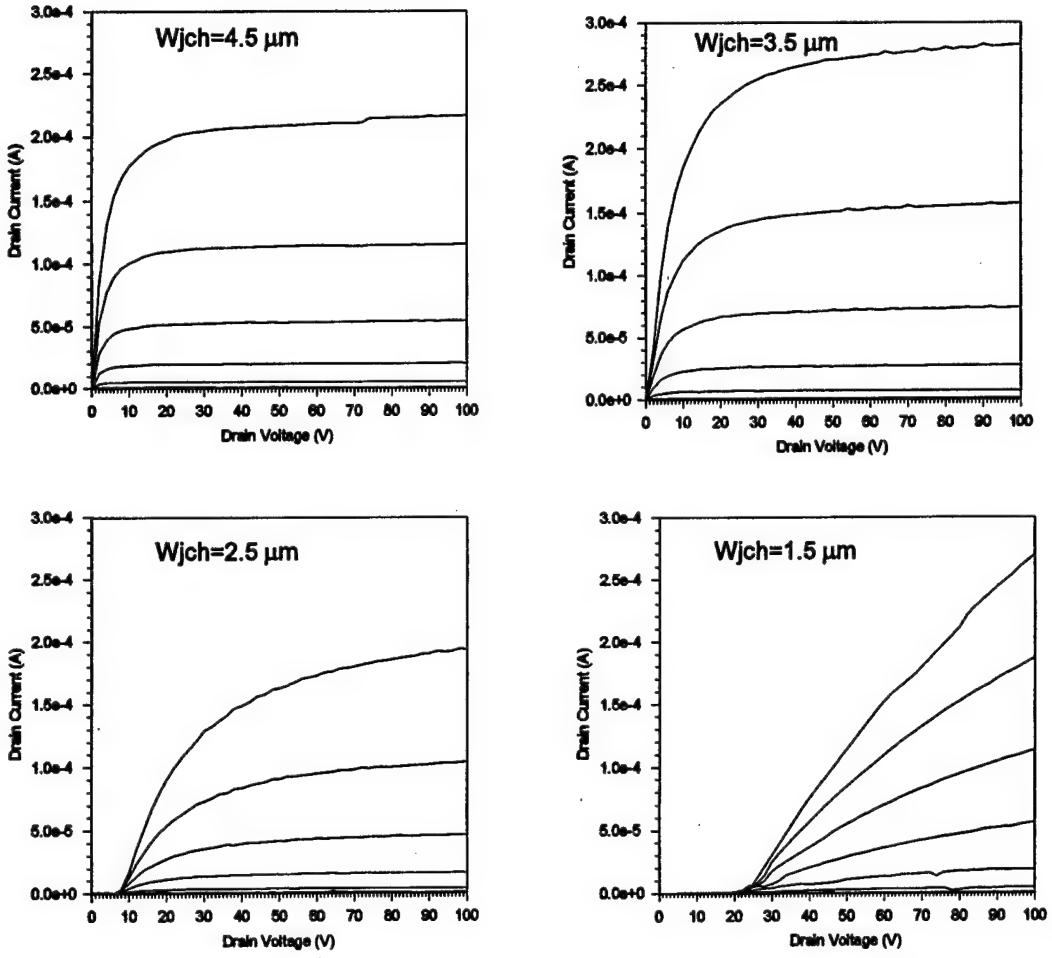

Fig. 1.43 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 1 on a 40 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

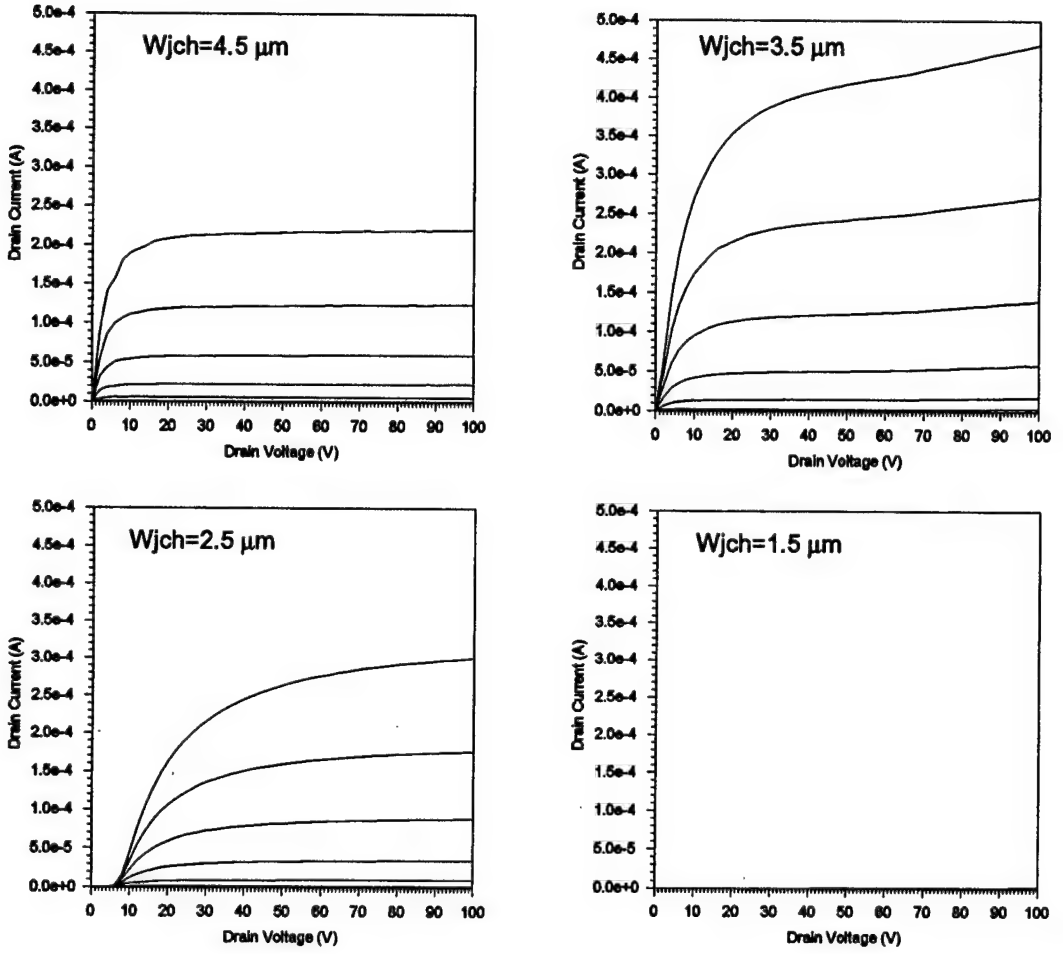

Fig. 1.44 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 2 on a 40 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

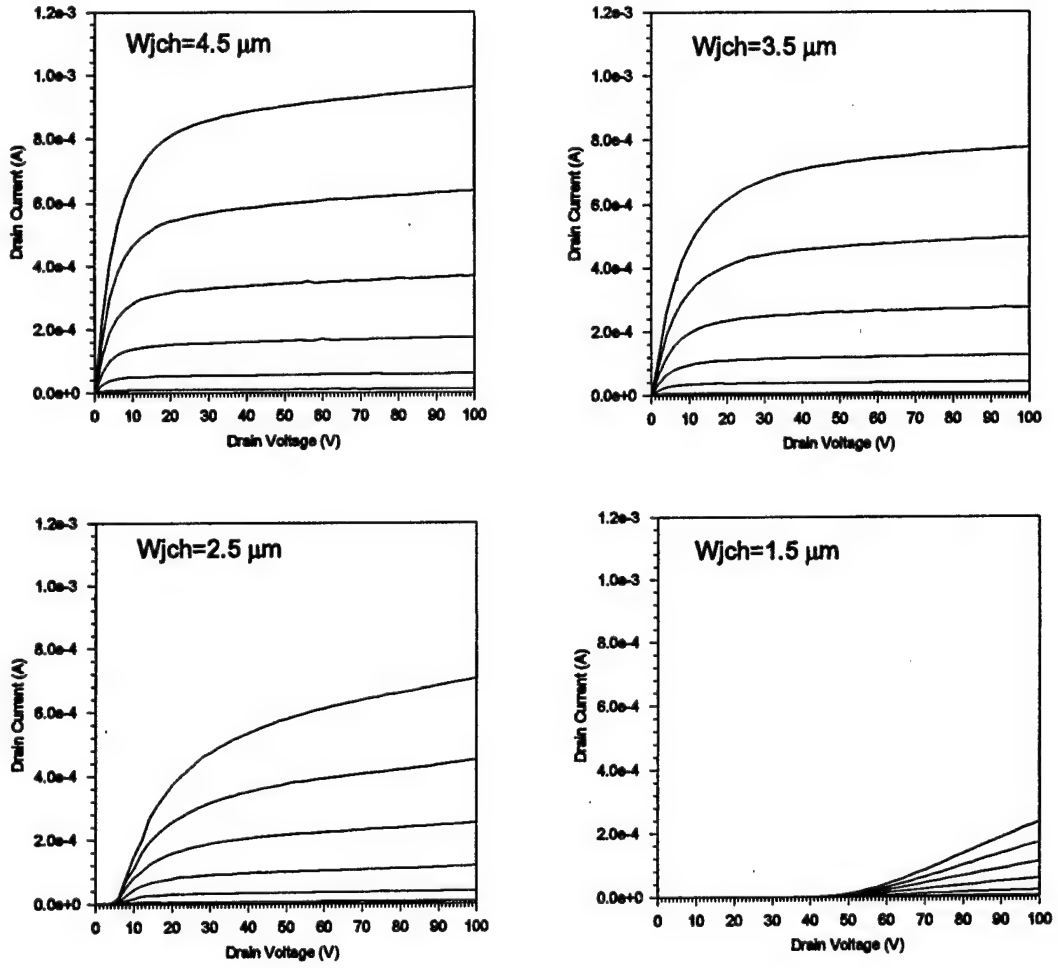

Fig. 1.45 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 3 on a 40 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

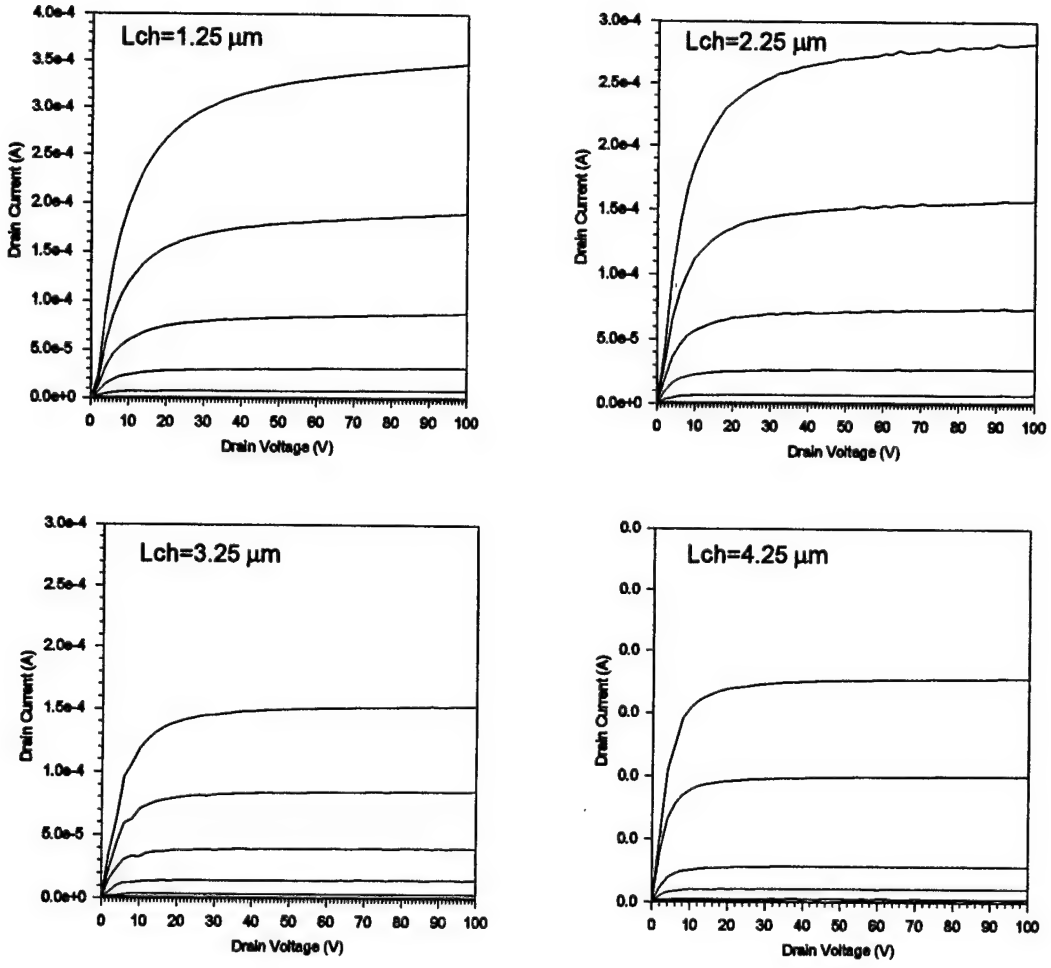

Fig. 1.46 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 1 on a 40 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

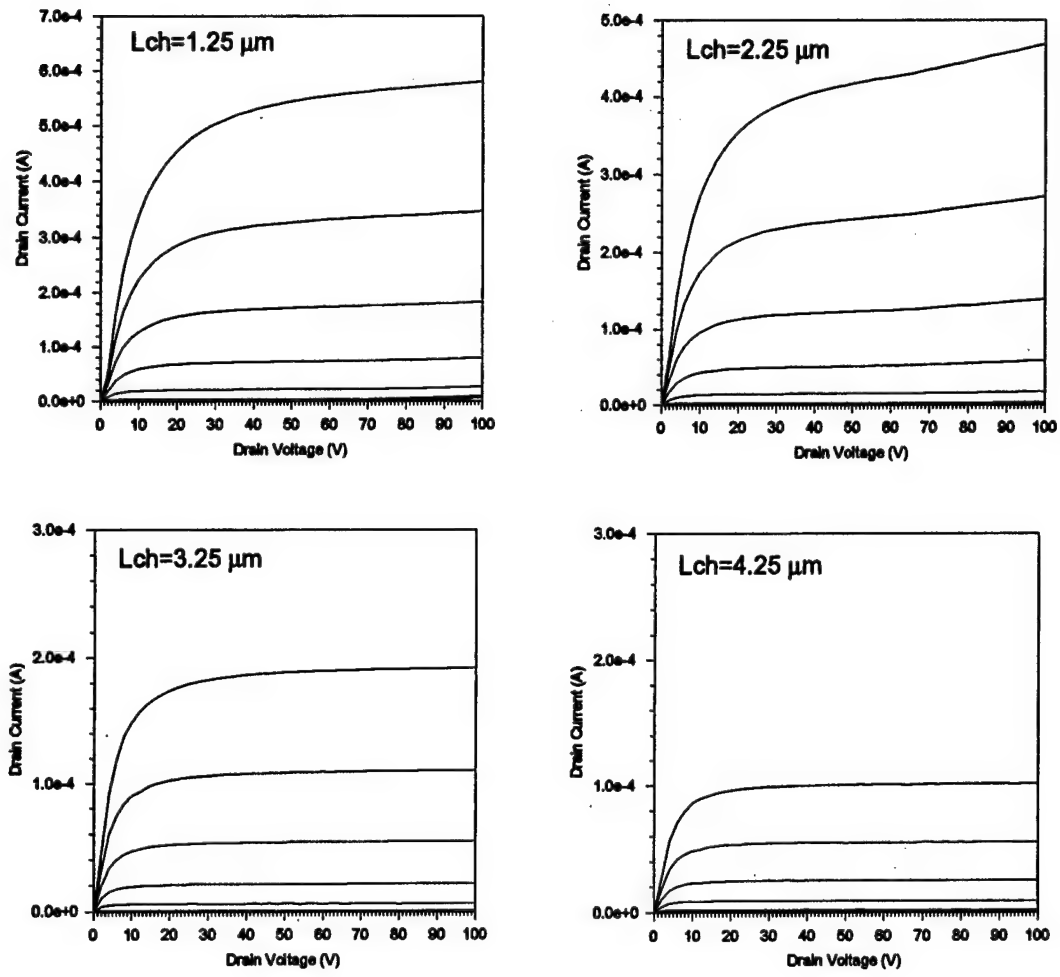

Fig. 1.47 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 2 on a 40 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

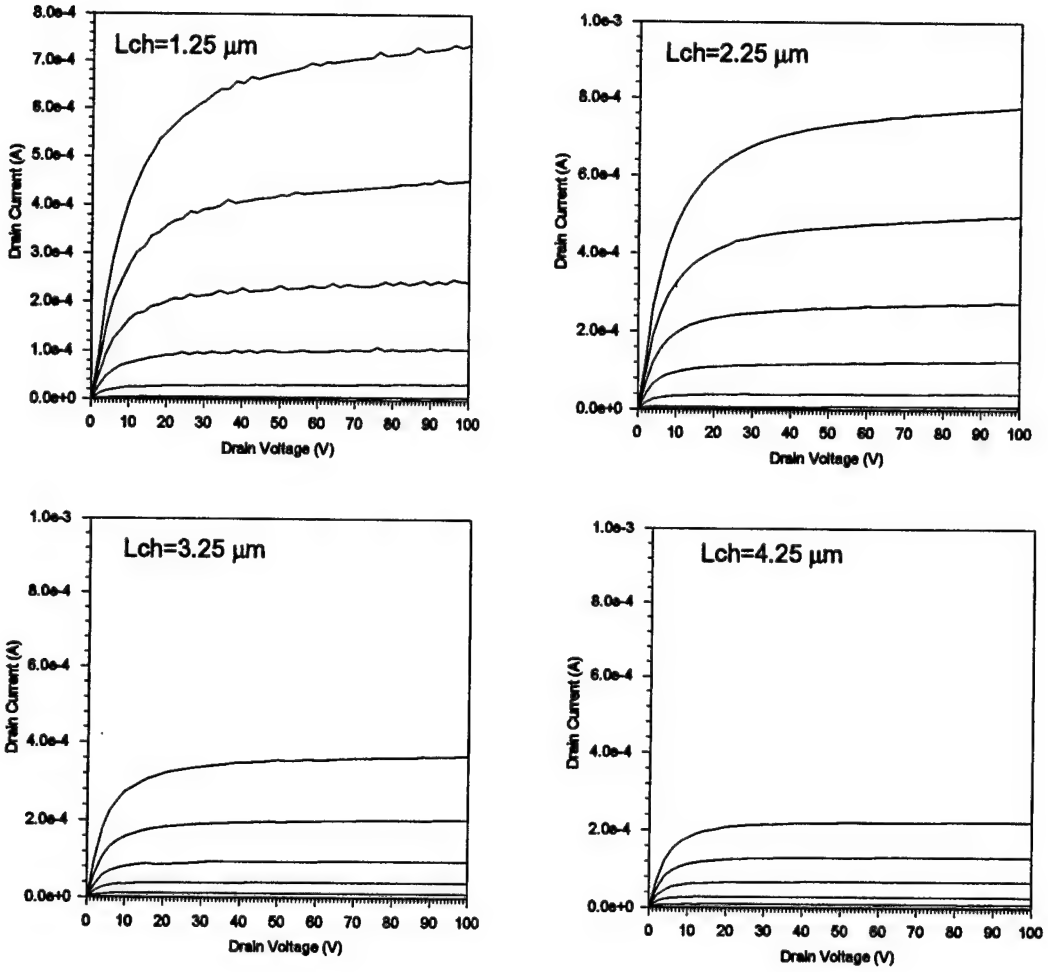

Fig. 1.48 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 3 on a 40 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at room temperature (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

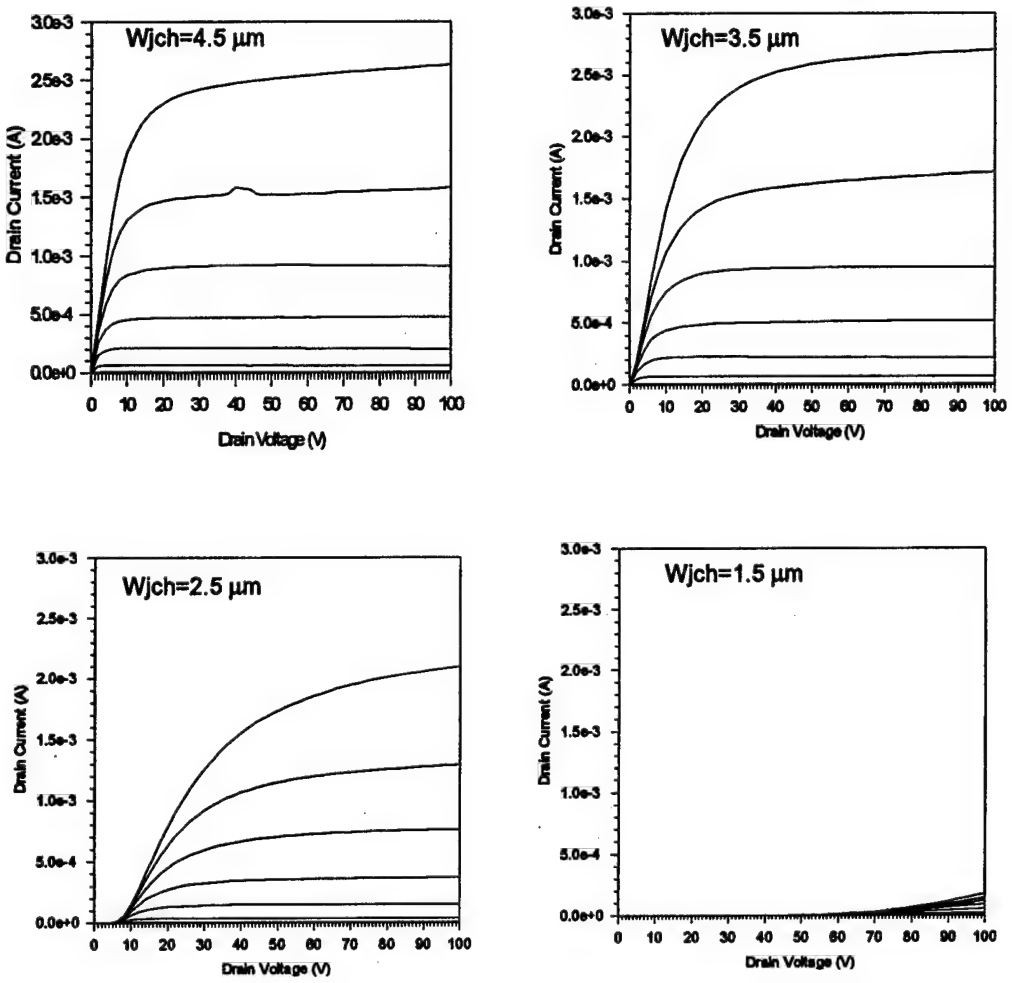

Fig. 1.49 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 1 on a 40 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

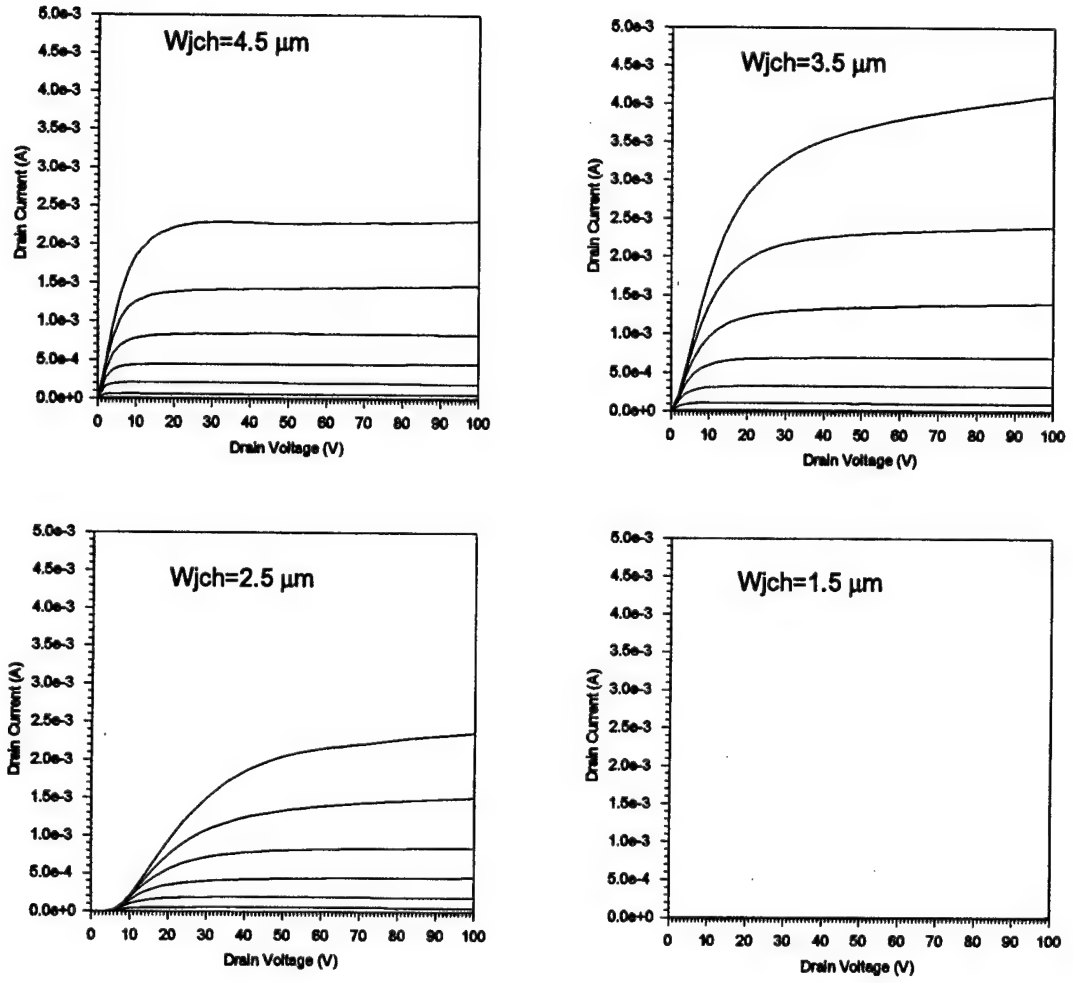

Fig. 1.50 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 2 on a 40 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

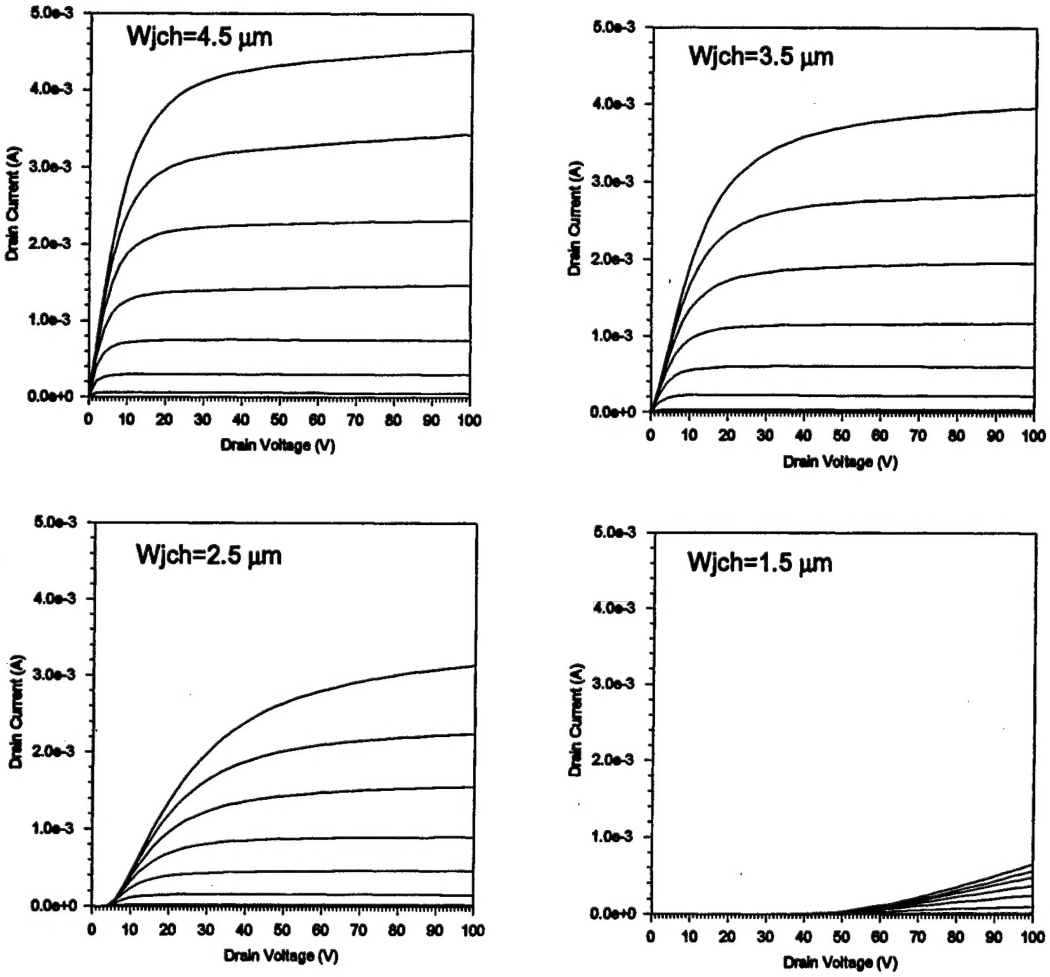

Fig. 1.51 Effect of the width of the buried JFET region (W_{jch}) on the output characteristics of an ACCUFET of device structure 3 on a 40 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, L_{ch}=2.25 µm)

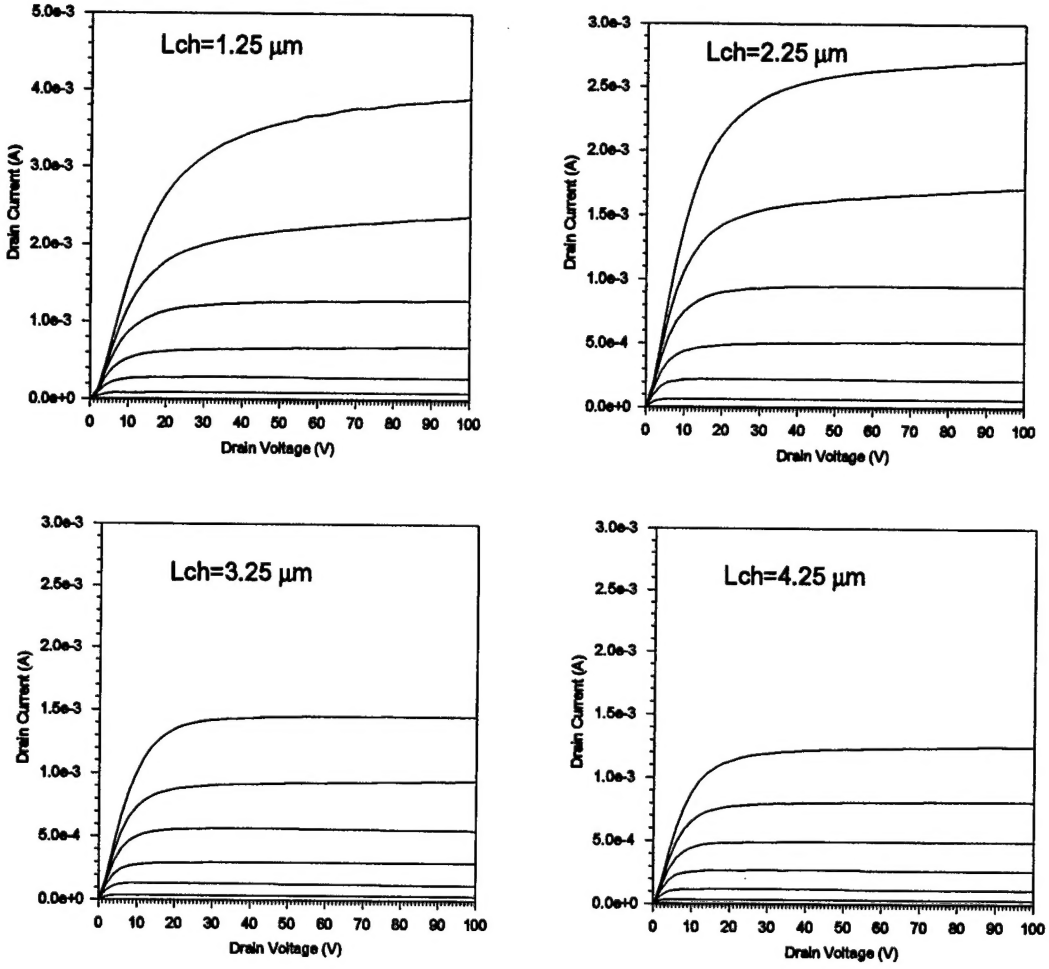

Fig. 1.52 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 1 on a 40 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

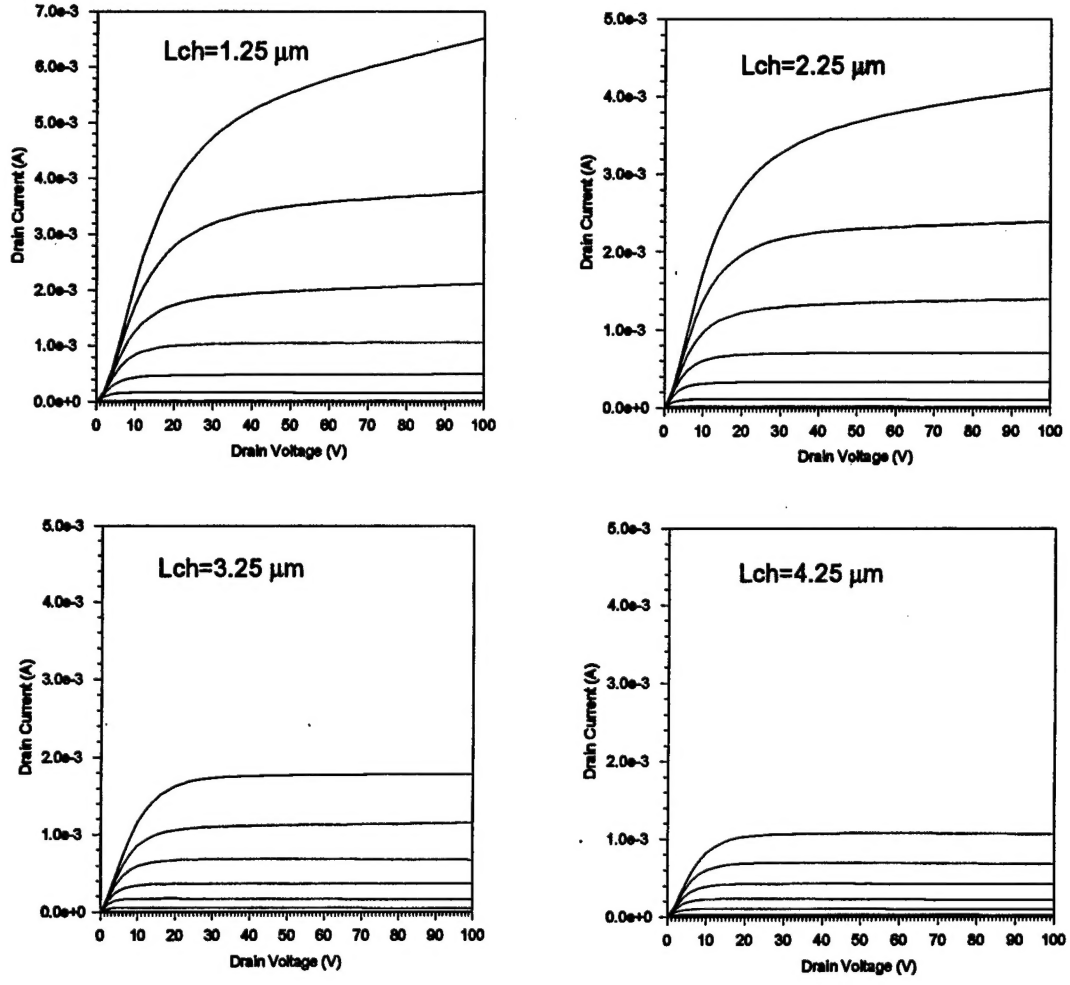

Fig. 1.53 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 2 on a 40 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)

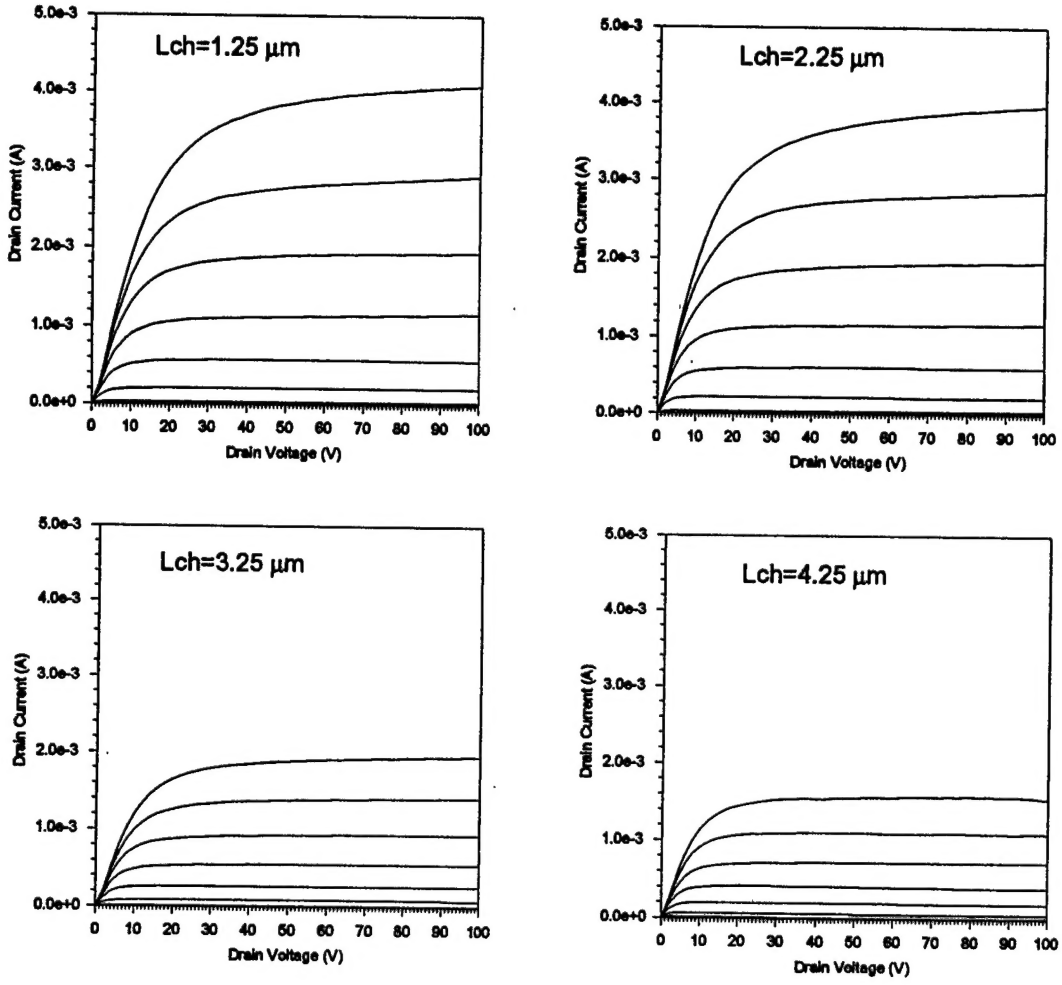

Fig. 1.54 Effect of the channel length (L_{ch}) on the output characteristics of an ACCUFET of device structure 3 on a 40 µm thick epilayer with a doping of $2x10^{15}$ cm^{-3} at 200 °C (gate voltage varied from 0 to 32 V in steps of 4 V). (LPCVD gate oxide, W_{jch}=3.5 µm)